2007 Paper 9 Question 3

VLSI Design

(*a*) What is meant by *dual-rail* logic? When is it used? [4 marks]

(*b*) Describe the purpose and operation of a Muller C element. [3 marks]

(*c*) Sketch a transistor-level circuit for a 3-input C element in CMOS, including an inverted output. [3 marks]

(*d*) Consider the design of a one-bit full-adder in asynchronous dual-rail logic. There will be three input pairs: (P_0, P_1), (Q_0, Q_1) and (R_0, R_1), and two output pairs: (S_0, S_1) for the high-order bit of the sum and (T_0, T_1) for the low-order bit. All inputs should become valid before any outputs become valid, and then all the outputs should remain valid until all the inputs are clear again. Sketch a circuit diagram for the adder using inverters, NAND gates, NOR gates and C elements. [10 marks]