2004 Paper 11 Question 3

Digital Electronics

An up–down binary counter is required. There is one control input (A) and a clock (CLK). The outputs are to be labelled D0, D1 and D2. If A=1 then the counter counts up every clock period, if A=0 it counts down. Design this counter in terms of AND, OR and XOR gates, and D flip-flops. Provide equations for the outputs and a circuit diagram of the complete system. [20 marks]