1999 Paper 8 Question 4

Comparative Architectures

A new microprocessor has a 64 Kbyte write-back L1 D-cache that is 2-way set-associative (employing a random replacement policy) with 64-byte cache lines. How might knowledge of these cache parameters be exploited in order to improve program performance? [5 marks]

What pros and cons might the designers have considered when selecting the cache line size? [5 marks]

The processor's L1 D-cache is indexed by virtual address and tagged by physical address. Why would the designers have done this? The processor has an 8 Kbyte page size, and so their decision is likely to have impact on the operating system virtual memory system. Explain why this is so, and state why the designers may have considered the possibility of increasing the cache's associativity. [5 marks]

The processor's physical address space is 64 bits wide. Calculate the number of bits of RAM required to implement the D-cache, including tag, data and status bits. [5 marks]