Consider the following Verilog phrases:

\[
\begin{align*}
\text{initial} & \quad r = 0; \\
\text{always \@(posedge clk)} & \quad r = a + r;
\end{align*}
\]

Write down a formula in logic that relates \( \text{clk} \), \( a \) and \( r \) at a level of abstraction where clock edges are explicitly represented. \([4 \text{ marks}]\)

Write down a second formula that models only the sequences of values of \( a \) and \( r \) at successive clock cycles. \([4 \text{ marks}]\)

Discuss the relationship between the two formulae. \([4 \text{ marks}]\)

Formalise and prove, using your second formula, that on the \( n^{th} \) cycle the value of \( r \) is the sum of the values of \( a \) on all the cycles up to the \( n^{th} \). You may assume that values are natural numbers and ignore the possibility of overflow. \([8 \text{ marks}]\)