1999 Paper 12 Question 2

Computer Design

instruction fetch	decode/ register fetch	execute	memory access	register write back

With reference to the classic RISC pipeline above, explain what a branch delay slot is and why it arises. [5 marks]

Demonstrate how conditional instructions can be used to avoid branches by writing code excerpts to perform the following function using a register-based processor. Comment your code to explain instruction semantics.

```
fun max(a,b) = if a>b then a else b;
```
[5 marks]

To assist with subroutine calls, ARM processors have a branch-with-link instruction and Intel processors have a call instruction. How do these instructions differ from a simple branch? [5 marks]

What is an *interrupt* and how is it similar to a branch-with-link instruction on the ARM? [5 marks]