Digital Electronics

You are to design a circuit with the following inputs:

- \( D \) – the data input
- \( R \) – a reset input (active high)
- \( CLK \) – a clock

and one output, \( ERR \).

\( ERR \) should be high if an error is found. An error occurs if, since the last reset, in the sequence of \( D \) values which occur on the rising edge of the clock the number of zeros exceeds the number of ones by three, or \textit{vice versa}. \( R \) should be sampled on the rising edge of the clock. When \( R \) is asserted, the \( D \) value is ignored.

\( (a) \) Give a state diagram for the circuit. [10 marks]

\( (b) \) Implement the circuit using J-K flip flops. [10 marks]