

1997 Paper 7 Question 3

Comparative Architectures

You are a computer architect working on the design of your company's new instruction set architecture for the 21st Century. Analysis of the latest implementation of the current architecture indicates that removal of logic to perform 8- and 16-bit loads and stores could result in a 20% reduction in processor cycle time. You have been assigned to assess the overall performance implications of removing sub-word memory accesses from the current architecture in order to determine whether they will be omitted from the new architecture.

First, you need to consider what sequence of instructions will be required to emulate sub-word loads and stores in software using standard instructions. Show the instruction sequences that will be required to load and store a *signed byte* value given an arbitrary byte address stored in a register. Be sure to state any assumptions you make. [10 marks]

Here is a summary of some dynamic instruction mix data that have been collected from the company's current processor executing an important integer benchmark:

| Instruction | Percentage | Instruction | Percentage |
|-------------|------------|-------------|------------|
| load | 20% | add | 18% |
| branch | 16% | compare | 13% |
| store | 9% | or | 8% |
| shift | 7% | other | 9% |

Of the loads and stores, 94% are 32-bit, 0% are 16-bit, and 6% are 8-bit. Assuming that your instruction sequences are used to replace all the 8-bit memory accesses, estimate the overall performance of the new implementation relative to the one with hardware support for such accesses. [4 marks]

In practice, shorter instruction sequences can be used to replace most sub-word accesses on processors without such hardware support. What extra instruction set features or compiler optimisations might be used to reduce the overhead of sub-word memory accesses? [6 marks]