1996 Paper 7 Question 11

Specification and Verification II

Explain how a register can be modelled either as a unit-delay, or with an explicit clock input. [4 marks]

Describe the relationship between the two models. [4 marks]

Design a device with input i and output o that outputs on o the sum of the inputs present at i at the preceding two clock edges. [4 marks]

Give two specifications of the device: (a) as an abstract sequential machine and (b) with an explicit clock input. [4 marks]

State a logical relationship between the two specifications. [4 marks]