

1995 Paper 7 Question 2

VLSI

Give the transistor level design of a CMOS static 2-input NAND gate. [7 marks]

Sketch the layout of this gate either using stick diagrams or by showing the diffusion, polysilicon, and metal areas. [8 marks]

How could the characteristics of your design be altered to drive large loads in a symmetric way? [5 marks]