Processor Architecture

A classical RISC five-stage pipeline is depicted below:

<table>
<thead>
<tr>
<th>Instruction fetch</th>
<th>Register fetch</th>
<th>Execute</th>
<th>Memory access</th>
<th>Register write back</th>
</tr>
</thead>
</table>

Using the above pipeline as a basis for discussion, explain the following:

(a) What are *data bypasses* (sometimes called feed-forward paths)? [5 marks]

(b) The above pipeline is likely to have two bypasses. Between which stages are the bypasses required and why? [5 marks]

(c) Why do load delay slots arise? [5 marks]

(d) Which of the following code segments will execute more quickly on the above pipeline and why (you may assume that there are no cache misses)?

<table>
<thead>
<tr>
<th>Code segment 1</th>
<th>Code segment 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>load r1,4(sp)</td>
<td>load r1,4(sp)</td>
</tr>
<tr>
<td>load r2,8(sp)</td>
<td>load r2,8(sp)</td>
</tr>
<tr>
<td>load r3,12(sp)</td>
<td>load r3,12(sp)</td>
</tr>
<tr>
<td>add r1,r2,r4 # r4=r1+r2</td>
<td>add r2,r3,r4 # r4=r2+r3</td>
</tr>
<tr>
<td>add r3,r4,r4 # r4=r3+r4</td>
<td>add r1,r4,r4 # r4=r1+r4</td>
</tr>
</tbody>
</table>

[5 marks]