1995 Paper 5 Question 1

Processor Architecture

A classical RISC five-stage pipeline is depicted below:

instruction fetch	register fetch	execute	memory access	register write back

Using the above pipeline as a basis for discussion, explain the following:

(a) What are *data bypasses* (sometimes called feed-forward paths)? [5 marks]

(b) The above pipeline is likely to have two bypasses. Between which stages are the bypasses required and why? [5 marks]

(c) Why do load delay slots arise? [5 marks]

(d) Which of the following code segments will execute more quickly on the above pipeline and why (you may assume that there are no cache misses)?

Code segment 1

```
load r1,4(sp)
load r2,8(sp)
load r3,12(sp)
add r1,r2,r4 # r4=r1+r2
add r3,r4,r4 # r4=r3+r4
```

Code segment 2

```
load r1,4(sp)
load r2,8(sp)
load r3,12(sp)
add r2,r3,r4 # r4=r2+r3
add r1,r4,r4 # r4=r1+r4
```

[5 marks]