

IA – Digital Electronics

Examples Paper 3 – FSMs, Electronics and Processor Architecture

1. Eliminate the redundant states from the following state table using the Row Matching approach

Current State	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	G	F	0	1
G	A	F	0	1

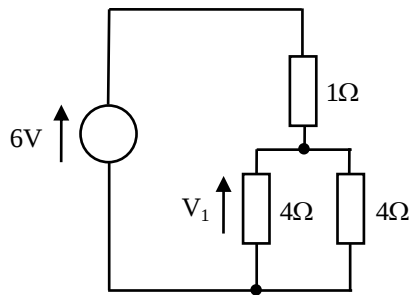
2. Eliminate the redundant states from the following state table using the State Equivalence/Implication Table approach

Current State	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
S ₀	S ₃	S ₃	1	1
S ₁	S ₂	S ₂	1	0
S ₂	S ₁	S ₁	1	1
S ₃	S ₀	S ₂	1	0

3. Eliminate the redundant states from the following state table using the State Equivalence/Implication Table approach

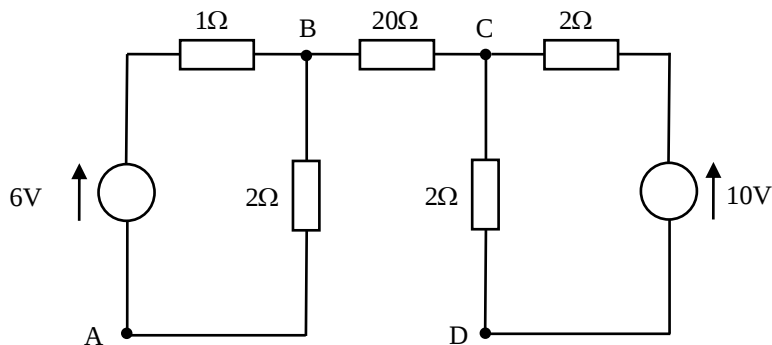
Current State	Next State				Output (Z)
	XY= 00	01	10	11	
S ₀	S ₀	S ₁	S ₂	S ₃	1
S ₁	S ₀	S ₃	S ₁	S ₅	0
S ₂	S ₁	S ₃	S ₂	S ₄	1
S ₃	S ₁	S ₀	S ₄	S ₅	0
S ₄	S ₀	S ₁	S ₂	S ₅	1
S ₅	S ₁	S ₄	S ₀	S ₅	0
S ₆	S ₄	S ₁	S ₂	S ₃	1

4. For the following circuit:



- What is the current through the 1Ω resistor?
- What is voltage V_1 ?
- What power is dissipated in each of the 4Ω resistors?

5. For the following circuit:



- What is the current flowing through the 20Ω resistor?
- Find the voltage at nodes B, C, and D with respect to node A, i.e., V_{AB} , V_{AC} and V_{AD} .

6. The n-MOS FET with the characteristics shown in Fig. 1(b) is used to implement the inverter circuit shown in Fig. 1(a).

- Draw a load line (i.e., resistor characteristic) on Fig. 1(b) and determine the output voltage V_o , corresponding to input voltages V_i , of 0V and 10V.
- Calculate the power dissipated in the 500Ω resistor and the transistor for each input voltage.

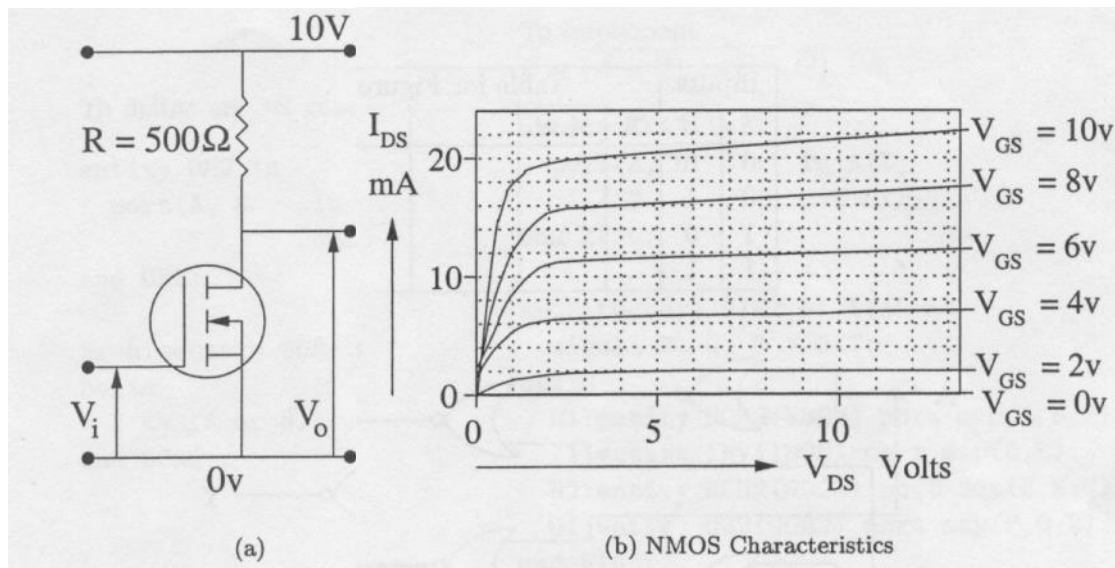


Figure 1:

7. (a) Explain the terms architecture and microarchitecture when applied to a processor.
- (b) Show how the microarchitecture of a simple single cycle processor can be modified to permit data memory access.
- (c) Show how the microarchitecture of a simple cycle processor can be modified to permit branching.
- (d) What are the main advantages of a multicycle processor over a single cycle processor?
- (e) How does a pipelined processor improve performance compared to a multicycle processor?

Relevant IA Paper 2 Tripos questions include: Q2-2023, Q2-2021, Q2-2019, Q2-2015, Q2-2012 (excluding rise and fall time calculations).