IA – Digital Electronics

Examples Paper 3 – FSMs, Electronics and Processor Architecture

1. Eliminate the redundant states from the following state table using the Row Matching approach

Current State	Next State X=0	Next State X=1	Output (Z) X=0	Output (Z) X=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	G	F	0	1
G	A	F	0	1

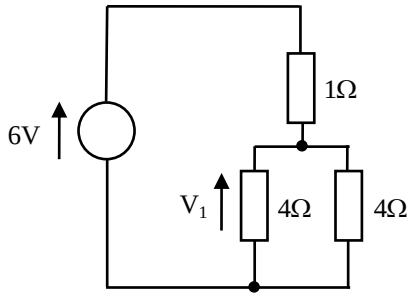
2. Eliminate the redundant states from the following state table using the State Equivalence/Implication Table approach

Current State	Next State X=0	Next State X=1	Output (Z) X=0	Output (Z) X=1
S_0	S_3	S_3	1	1
S_1	S_2	S_2	1	0
S_2	S_1	S_1	1	1
S_3	S_0	S_2	1	0

3. Eliminate the redundant states from the following state table using the State Equivalence/Implication Table approach

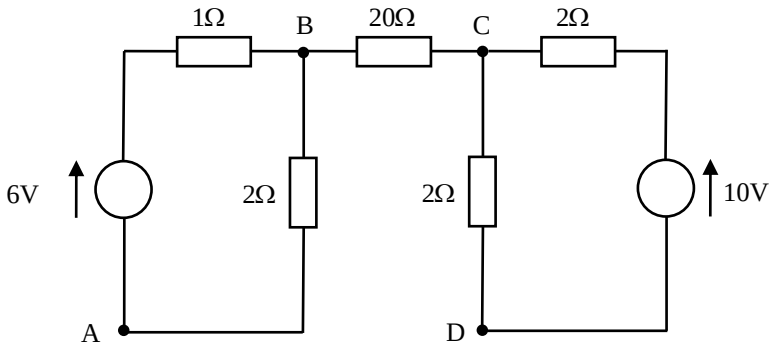
Current State	Next State XY= 00	01	10	11	Output (Z)
S_0	S_0	S_1	S_2	S_3	1
S_1	S_0	S_3	S_1	S_5	0
S_2	S_1	S_3	S_2	S_4	1
S_3	S_1	S_0	S_4	S_5	0
S_4	S_0	S_1	S_2	S_5	1
S_5	S_1	S_4	S_0	S_5	0
S_6	S_4	S_1	S_2	S_3	1

4. For the following circuit:



(a) What is the current through the 1Ω resistor?
(b) What is voltage V_1?
(c) What power is dissipated in each of the 4Ω resistors?

5. For the following circuit:



(a) What is the current flowing through the 20Ω resistor?
(b) Find the voltage at nodes B, C, and D with respect to node A, i.e., V_{AB}, V_{AC} and V_{AD} .

6. The n-MOS FET with the characteristics shown in Fig. 1(b) is used to implement the inverter circuit shown in Fig. 1(a).

(a) Draw a load line (i.e., resistor characteristic) on Fig. 1(b) and determine the output voltage V_o, corresponding to input voltages V_i, of 0V and 10V.
(b) Calculate the power dissipated in the 500Ω resistor and the transistor for each input voltage.

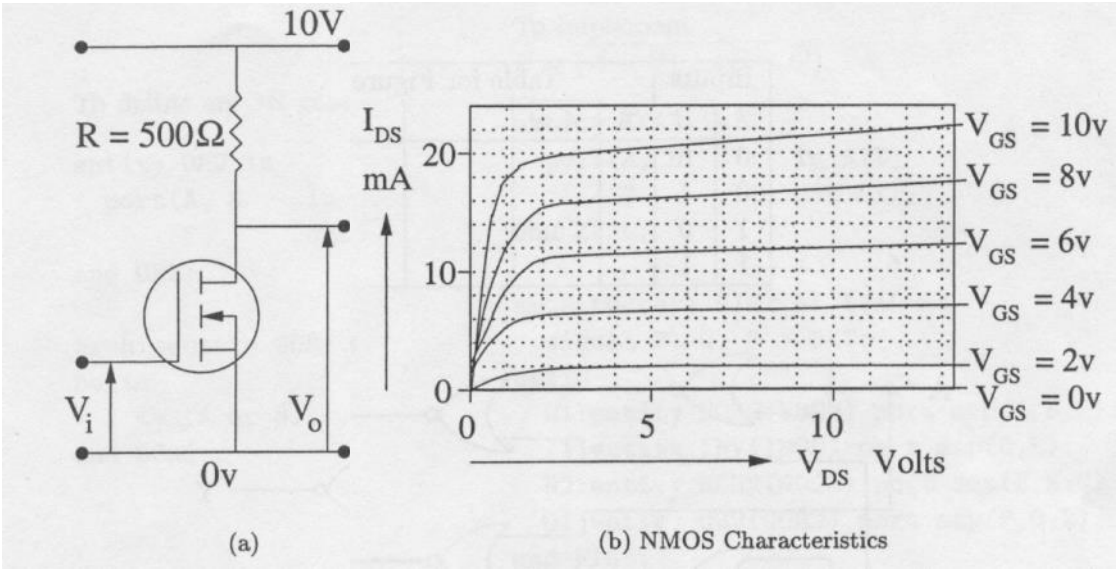


Figure 1:

7. (a) Explain the terms architecture and microarchitecture when applied to a processor.
(b) Show how the microarchitecture of a simple single cycle processor can be modified to permit data memory access.
(c) Show how the microarchitecture of a simple cycle processor can be modified to permit branching.
(d) What are the main advantages of a multicycle processor over a single cycle processor?
(e) How does a pipelined processor improve performance compared to a multicycle processor?

Relevant IA Paper 2 Tripos questions include: Q2-2023, Q2-2021, Q2-2019, Q2-2015, Q2-2012 (excluding rise and fall time calculations).

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