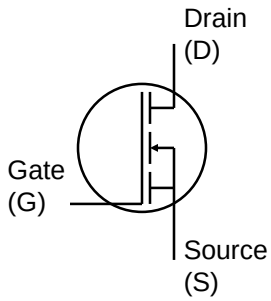
Digital Electronics: Electronics, Devices and Circuits

Transistors and Gates

n-Channel MOSFET

- We will now briefly introduce the n-channel MOSFET
- The charge carriers in this device are electrons

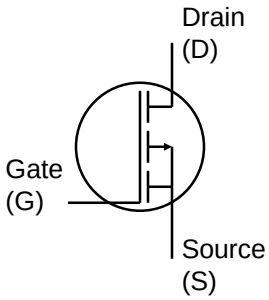


The current flow from D to S (I_{DS}) is controlled by the voltage applied between G and S (V_{GS}), i.e., G has to be +ve wrt S for current I_{DS} to flow (transistor **On**)

We will consider enhancement mode devices in which no current flows (I_{DS}=0, i.e., the transistor is **Off**) when V_{GS}=0V

p-Channel MOSFET

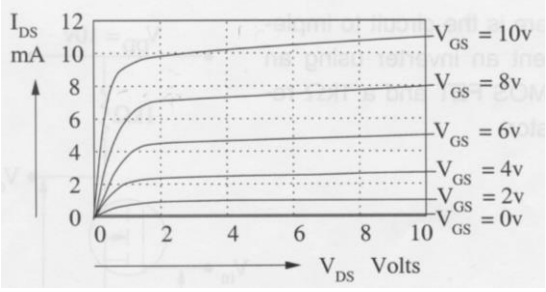
- Similarly we have p-channel MOSFETs where the charge carriers are holes



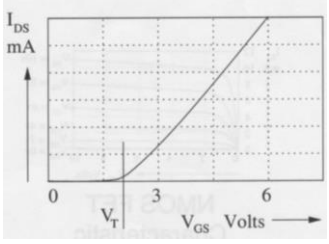
The current flow from S to D (I_{DS}) is controlled by the voltage applied between G and S (V_{GS}), i.e., G has to be -ve wrt S for current I_{DS} to flow (transistor **On**)

We will be consider enhancement mode devices in which no current flows (I_{DS}=0, i.e., the transistor is **Off**) when V_{GS}=0V

n-MOSFET Characteristics



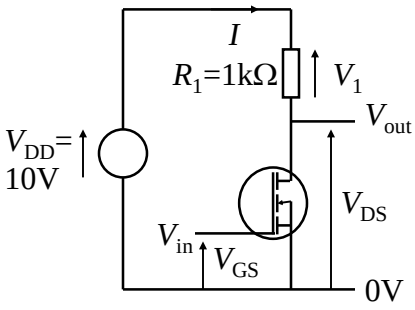
Plots V-I characteristics of the device for various Gate voltages (V_{GS})

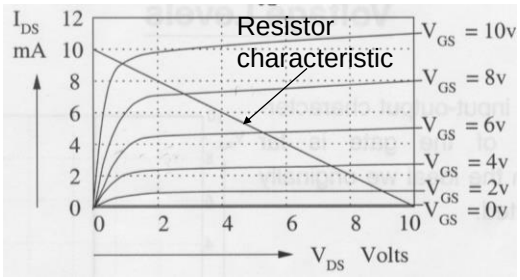


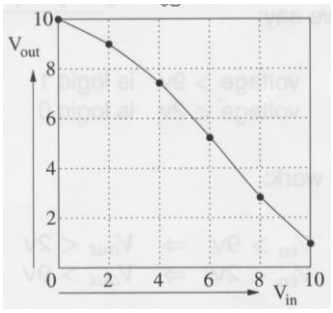
At a constant value of V_{DS} , we can also see that I_{DS} is a function of the Gate voltage, V_{GS}

The transistor begins to conduct when the Gate voltage, V_{GS} , reaches the Threshold voltage: V_T

n-MOS Inverter







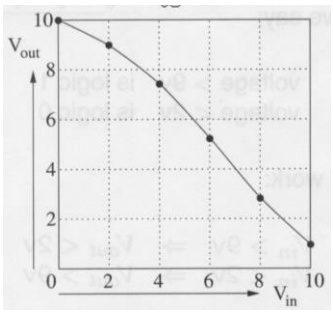
We can use the graphical approach to determine the relationship between V_{in} and V_{out}

Note $V_{in}=V_{GS}$ and $V_{out}=V_{DS}$

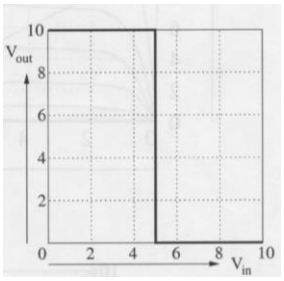
n-MOS Inverter

- Note it does not have the 'ideal' characteristic that we would like from an 'inverter' function

Actual



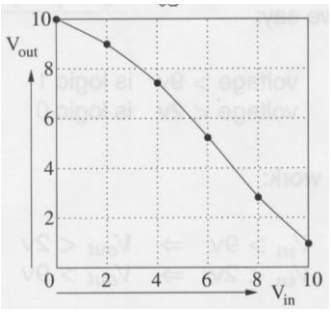
Ideal



However if we specify suitable voltage thresholds, we can achieve a 'binary' action.

n-MOS Inverter

Actual



So if we say:

voltage > 9V is logic 1

voltage < 2V is logic 0

The gate will work as follows:

V_{in} > 9V then V_{out} < 2V and if

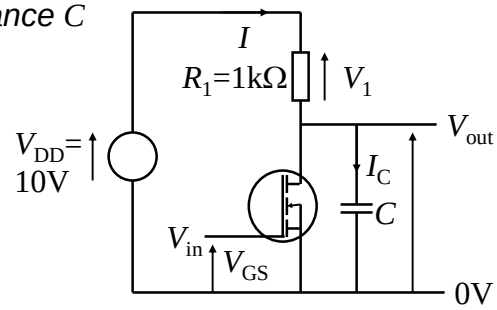
V_{in} < 2V then V_{out} > 9V

n-MOS Logic

- It is possible (and was done in the early days) to build other logic functions, e.g., NOR and NAND using n-MOS transistors
- However, n-MOS logic has fundamental problems:
  - Speed of operation
  - Power consumption

n-MOS Logic

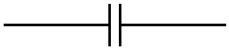
- One of the main speed limitations is due to stray capacitance owing to the metal track used to connect gate inputs and outputs. This has a finite capacitance to ground, i.e., the 0V connection.
  - We modify the circuit model to include this *stray capacitance C*



- To see the effect of stray capacitance, we first consider the electrical properties of capacitors.

Devices that store energy

- Some common circuit components store energy, e.g., capacitors and inductors.
- We will now consider capacitors in detail.
- The physical construction of a capacitor is effectively 2 conductors separated by a non-conductor (or dielectric as it is known).



Symbol of a Capacitor

Unit of capacitance: Farads (F)

- Electrical charge can be stored in such a device.

Capacitors

- So, parallel conductors brought sufficiently close (but not touching) will form a capacitor
- Parallel conductors often occur on circuit boards (and on integrated circuits), thus creating unwanted (or parasitic) capacitors.
- We will see that parasitic capacitors can have a significant negative impact on the switching characteristics of digital logic circuits.

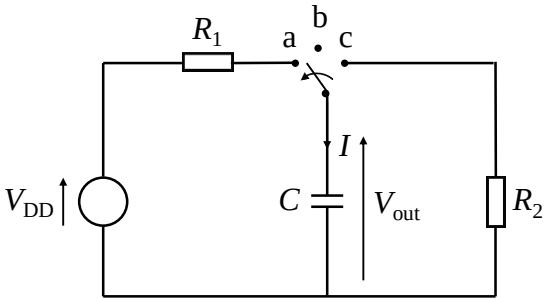
Capacitors

- The relationship between the charge Q stored in a capacitor C and the voltage V across its terminals is $Q = VC$.
- As mentioned previously, current is the rate of flow of charge, i.e., $\mathrm{d}Q/\mathrm{d}t = I$, or alternatively, $Q = \int Idt$.
- So we can write,

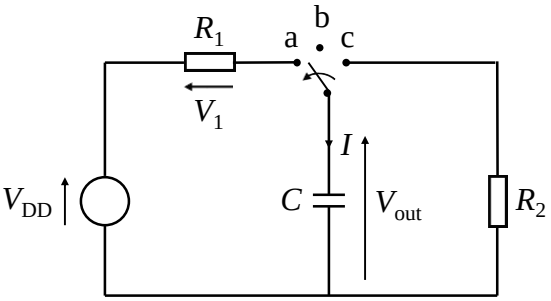
$$V = \frac{1}{C}\int Idt$$

Capacitors

- We now wish to investigate what happens when sudden changes in configuration occur in a simple resistor-capacitor (RC) circuit.

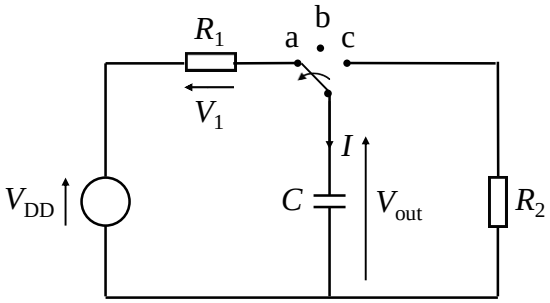


RC circuits



- Initially, C is discharged, i.e., $V_{out}=0$ and the switch moves from position b to position a
- C charges through R_1 and current I flows in R_1 and C

RC circuits



$$V_{DD} - V_1 - V_{out} = 0$$

$$V_{DD} = V_1 + V_{out}$$

Sub for V_{out} in terms of I and C (from earlier eqn.)

$$V_{DD} = IR_1 + \frac{1}{C}\int I dt$$

Differentiate wrt t gives

$$0 = R_1 \frac{dI}{dt} + \frac{I}{C}$$

Then rearranging gives $$-\frac{dt}{CR_1} = \frac{dI}{I}$$

RC circuits

Integrating both sides of the previous equation gives

$$-\frac{t}{CR_1} + a = \ln I$$

We now need to find the integration constant a .

To do this we look at the initial conditions at $t = 0$, i.e., $V_{out}=0$. This gives an initial current $I_0=V_{DD}/R_1$

$$a = \ln I_0 = \ln\left(\frac{V_{DD}}{R_1}\right)$$

So,

$$-\frac{t}{CR_1} + \ln I_0 = \ln I$$

$$-\frac{t}{CR_1} = \ln\frac{I}{I_0}$$

Antilog both sides,

$$e^{-t/CR_1} = \frac{I}{I_0}$$

$$I = I_0 e^{-t/CR_1}$$

RC circuits

Now,

$$V_{out} = V_{DD} - V_1$$

and,

$$V_1 = IR_1$$

Substituting for V_1 gives,

$$V_{out} = V_{DD} - IR_1$$

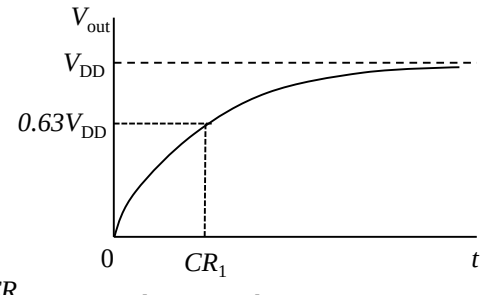
$$V_{out} = V_{DD} - R_1 I_0 e^{-t/CR_1}$$

Substituting for I_0 gives,

$$V_{out} = V_{DD} - R_1 \frac{V_{DD}}{R_1} e^{-t/CR_1}$$

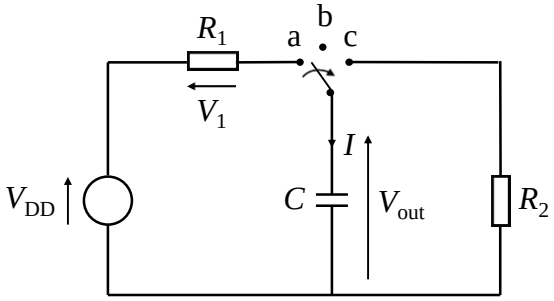
$$V_{out} = V_{DD}\left(1 - e^{-t/CR_1}\right)$$

Plotting yields,



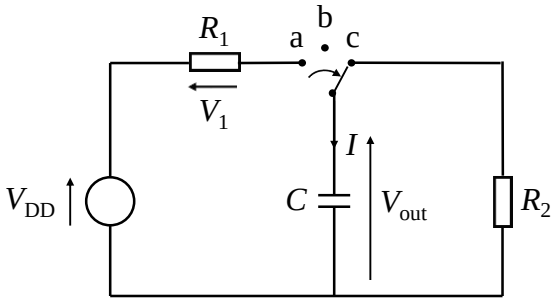
CR_1 is knows as the time constant – has units of seconds

RC circuits



- Initially assume C is fully charged, i.e., $V_{out}=V_{DD}$ and the switch moves from position a to position c
- C discharges through R_2 and current flows in R_2 and C

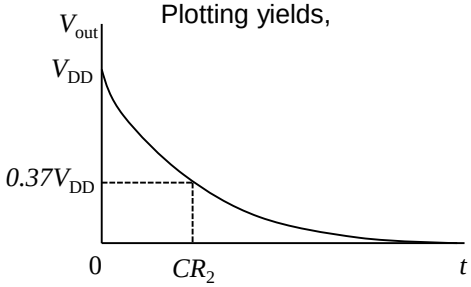
RC circuits



The expression for V_{out} is,

$$V_{out} = V_{DD} e^{-t/CR_2}$$

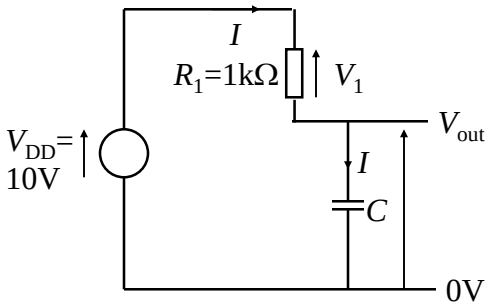
Plotting yields,



n-MOS Logic

- To see the effect of this stray capacitance we will consider what happens when the transistor is ON (so that V_{out}=0V at beginning), then turned OFF and then turned ON again
- When the transistor is OFF it is effectively an open circuit, i.e., we can eliminate if from the circuit diagram

Transistor turned OFF



The problem with capacitors is that the voltage across them cannot change instantaneously.

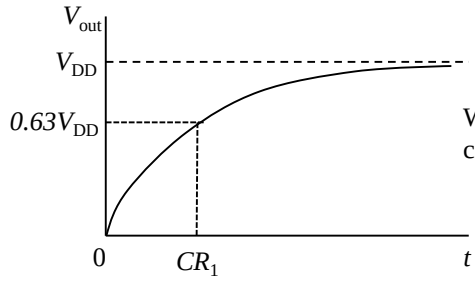
The 'stray' capacitor C charges through R_1. Note C is initially discharged, i.e., V_{out}=0V

n-MOS Logic

- Using the previous result for a capacitor charging via a resistor we can write:

$$V_{out} = V_{DD}\left(1 - e^{-t/CR_1}\right)$$

Plotting yields,

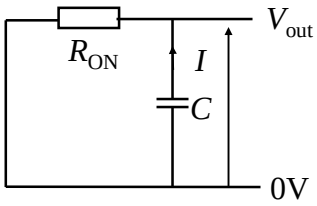


Where CR_1 is known as the time constant – has units of seconds

n-MOS Logic

- When the transistor is ON it is effectively a low value resistor, R_{ON}. (say < 100Ω)
- We will assume capacitor is charged to a voltage V_{DD} just before the transistor is turned ON

Transistor turned ON again

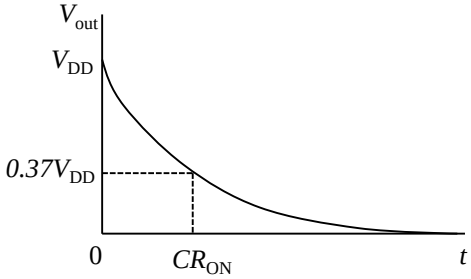


'Stray' capacitor C discharges through R_{ON}

The expression for V_{out} is,

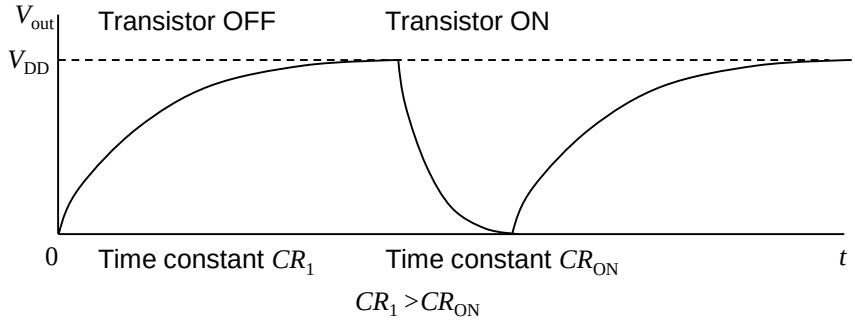
$$V_{out} = V_{DD}e^{-t/CR_{ON}}$$

Plotting yields,



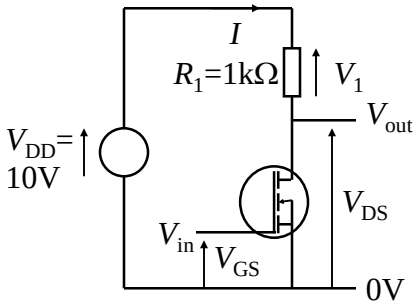
n-MOS Logic

- When the transistor turns OFF, C charges through R_1. This means the rising edge is slow since it is defined by the large time constant R_1C (since R_1 is high).
- When the transistor turns ON, C discharges through it, i.e., effectively resistance R_{ON}. The speed of the falling edge is faster since the transistor ON resistance (R_{ON}) is low.



n-MOS Logic

- Power consumption is also a problem



Transistor OFF

No problem since no current is flowing through R_1, i.e., V_{out} = 10V

Transistor ON

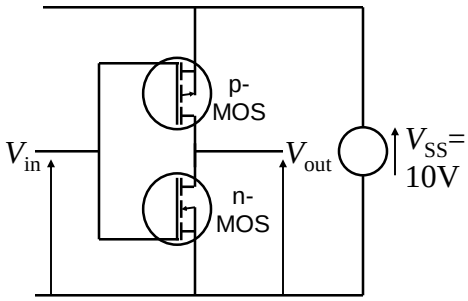
This is a problem since current is flowing through R_1 . For example, if V_{out} = 1V (corresponds with V_{in} = 10V and I_D = I = 9mA), the power dissipated in the resistor is the product of voltage across it and the current through it, i.e.,

$$P_{disp} = I \times V_1 = 9 \times 10^{-3} \times 9 = 81\,\text{mW}$$

CMOS Logic

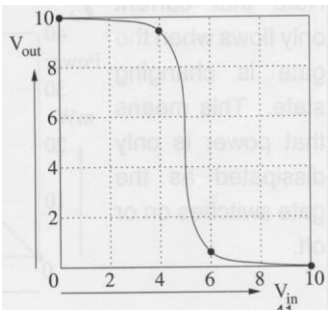
- To overcome these problems, complementary MOS (CMOS) logic was developed
- As the name implies it uses p-channel as well as n-channel MOS transistors
- Essentially, p-MOS transistors are n-MOS transistors but with all the polarities reversed!

CMOS Inverter



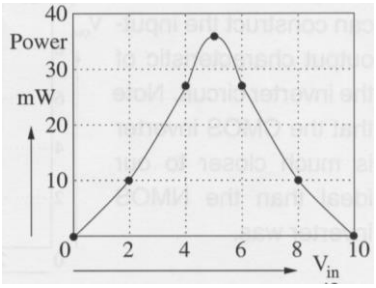
V_{in}	N-MOS	P-MOS	V_{out}
low	off	on	high
high	on	off	low

Using the graphical approach we can show that the switching characteristics are now much better than for the n-MOS inverter



CMOS Inverter

- It can be shown that the transistors only dissipate power while they are switching.



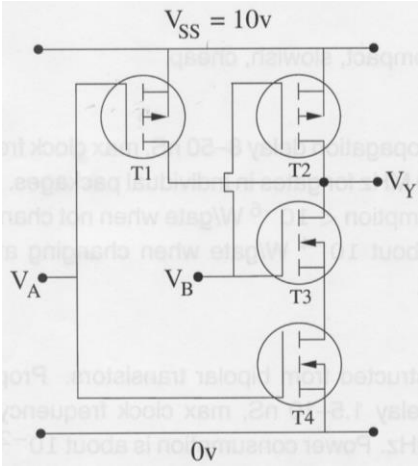
This is when both transistors are on. When one or the other is off, the power dissipation is zero

CMOS is also better at driving capacitive loads since it has active transistors on both rising and falling edges

CMOS Gates

- CMOS can also be used to build NAND and NOR gates
- They have similar electrical properties to the CMOS inverter

CMOS NAND Gate



V_A	V_B	T1	T2	T3	T4	V_Y
low	low	on	on	off	off	high
low	high	on	off	on	off	high
high	low	off	on	off	on	high
high	high	off	off	on	on	low

Logic Families

- **NMOS** – compact, slow, cheap, obsolete
- **CMOS** – Older families slow (4000 series about 60ns), but new ones (74AC) much faster (3ns). 74HC series popular
- **TTL** – Uses bipolar transistors. Known as 74 series. Note that most 74 series devices are now available in CMOS. Older versions slow (LS about 16ns), newer ones faster (AS about 2ns)
- **ECL** – High speed, but high power consumption

Logic Families

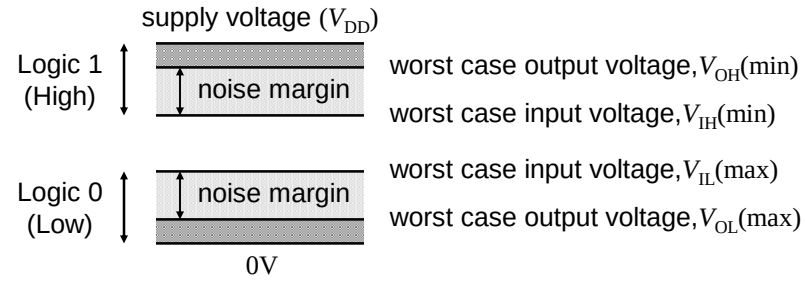
- Best to stick with the particular family which has the best performance, power consumption cost trade-off for the required purpose
- It is possible to mix logic families and sub-families, but care is required regarding the acceptable logic voltage levels and gate current handling capabilities

Meaning of Voltage Levels

- As we have seen, the relationship between the input voltage to a gate and the output voltage depends upon the particular implementation technology
- Essentially, the signals between outputs and inputs are ‘analogue’ and so are susceptible to corruption by additive noise, e.g., due to cross talk from signals in adjacent wires
- What we need is a method for quantifying the tolerance of a particular logic to noise

Noise Margin

- Tolerance to noise is quantified in terms of the noise margin



Logic 0 noise margin = V_{IL}(max) - V_{OL}(max)

Logic 1 noise margin = V_{OH}(min) - V_{IH}(min)

Noise Margin

- For the 74 series High Speed CMOS (HCMOS) used in the hardware labs (using the values from the data sheet):

Logic 0 noise margin = V_{IL}(max) - V_{OL}(max)

Logic 0 noise margin = 1.35 – 0.1 = 1.25 V

Logic 1 noise margin = V_{OH}(min) - V_{IH}(min)

Logic 1 noise margin = 4.4 – 3.15 = 1.25 V

See the worst case noise margin = 1.25V, which is much greater than the 0.4 V typical of TTL series devices. Consequently HCMOS devices can tolerate more noise pick-up before performance becomes compromised