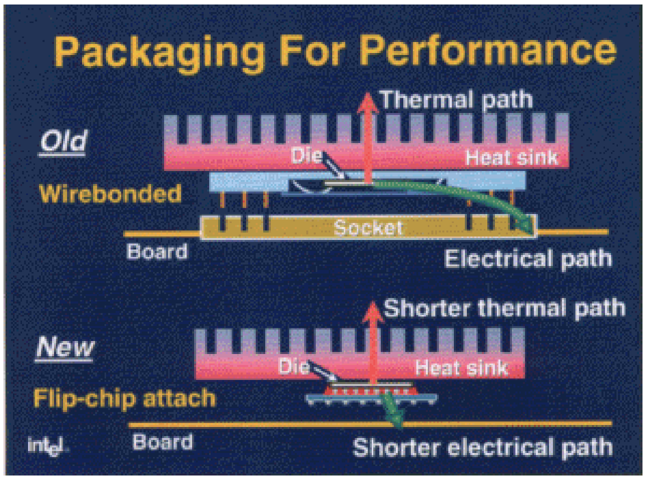
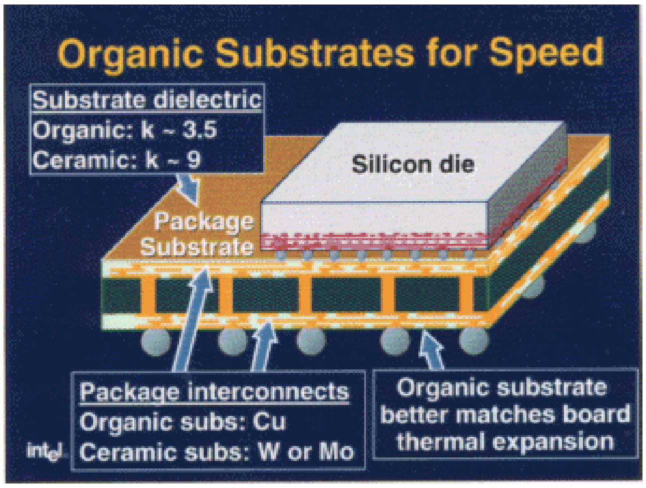
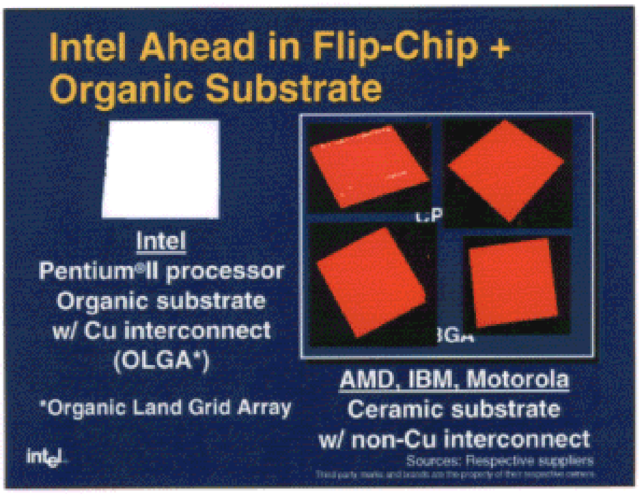
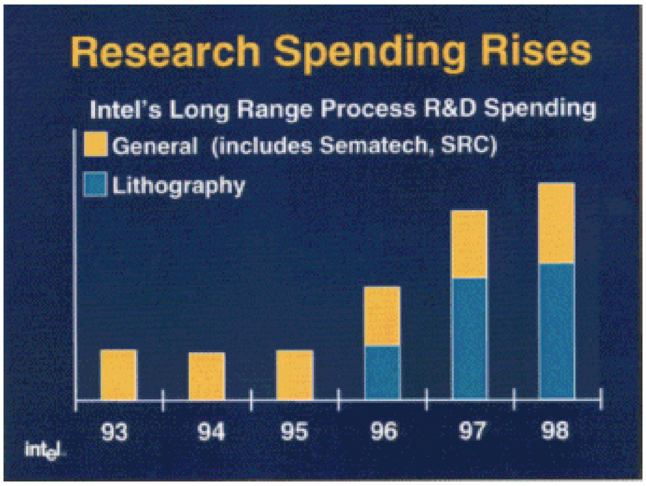
Posted 13/02/99 6:24pm by Mike Magee

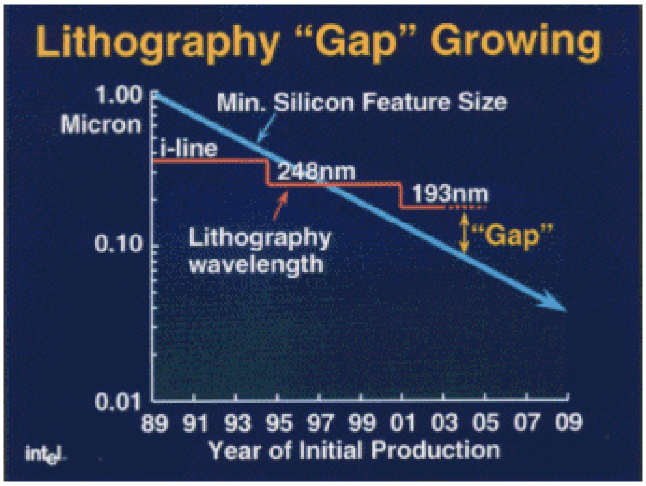
Intel's packaging and lithography plans

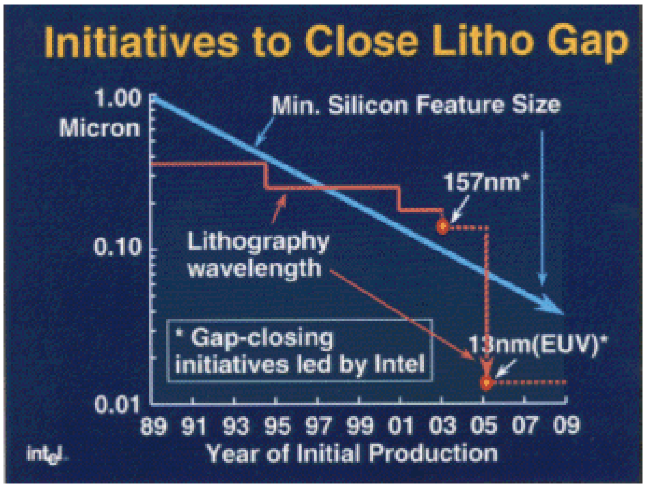








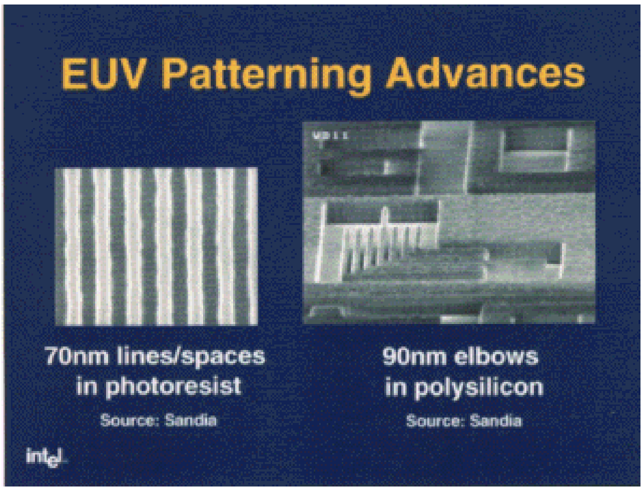


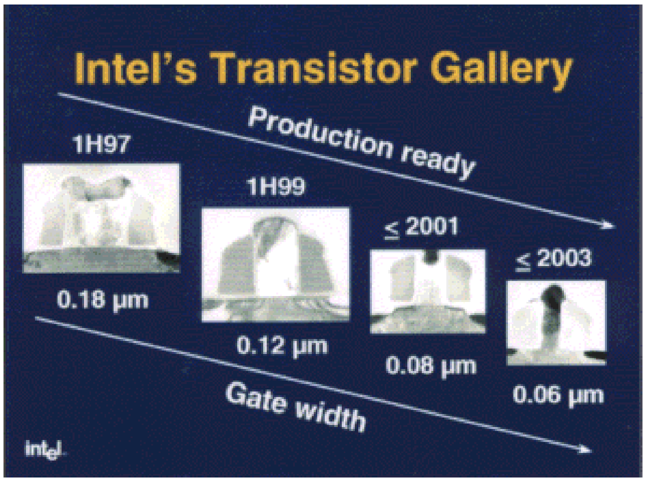


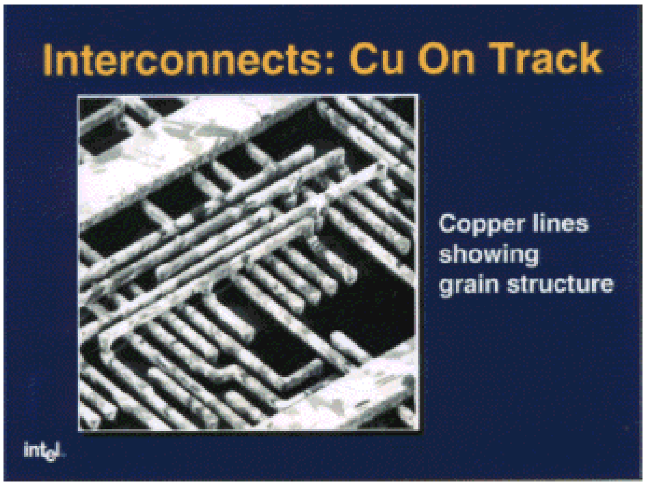
EUV: Eliminating The Gap

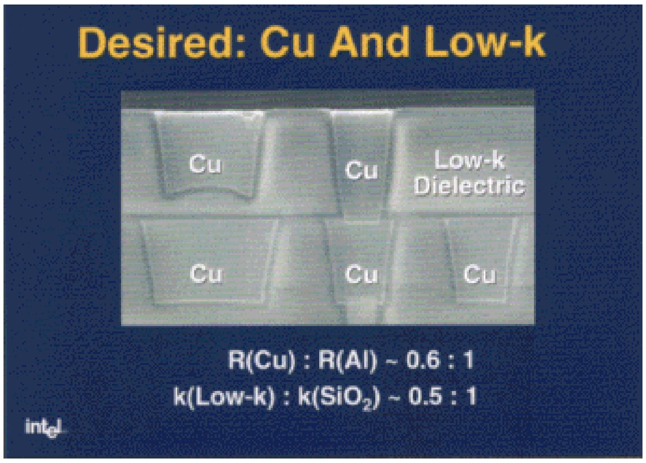
- EUV (Extreme Ultra Violet) lithography
  - 13nm wavelength
  - Reflective optics and masks
  - Scalable to limit of silicon technology
- EUV lithography R&D in U.S.
  - Funded by industrial consortium (EUV LLC)
  - 3 National Laboratories participating
  - Equipment and materials suppliers engaged
  - Selected by Sematech in 4Q98 as prime candidate for post-157nm lithography

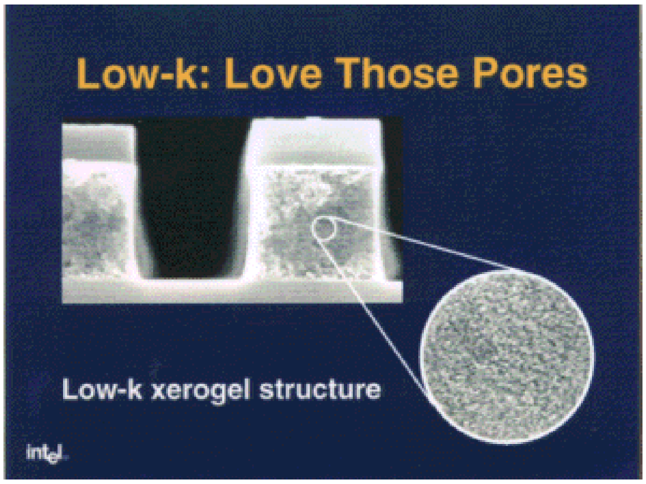
intel


EUV Patterning Advances
70nm lines/spaces in photoresist
Source: Sandia
90nm elbows in polysilicon
Source: Sandia
intel


Intel's Transistor Gallery
Production ready
1H97
0.18 µm
1H99
0.12 µm
≤ 2001
0.08 µm
≤ 2003
0.06 µm
Gate width
intel


Interconnects: Cu On Track
Copper lines showing grain structure
intel





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