P51: High Performance Networking
Proposed Projects

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1 Introduction

The following document provides some ideas for projects that can be taken as part of the course. Students are invited to propose their own projects, but other projects are subject to approval by the instructors. While the proposed projects are written in verilog, other languages and frameworks can be used as well. It is not a requirement for the project to run on NetFPGA.

All project proposals (including projects proposed in this document) need to be submitted via Moodle before the second lab session.
Due date: 30/1/2018, 16:00.

This document also contains the expected grading of the proposed projects. The noted marks are subject to the perfect completion of each stage. The grading of the projects will also refer to additional deliverables included as part of the project's documentation: architecture, performance profile, evaluation plan and evaluation results, etc.

2 High Bandwidth Switch

The goal of this project is to turn the NetFPGA $4 \times 10GE$ Reference Switch into $8 \times 10GE$ or $12 \times 10GE$.
Expected stages as grading:

- 80G switch (data path only), full line rate at all packet sizes (Mark: 60).
- 80G switch (data path only), with fair sharing BW between ports regardless of packet size and packet size mix. (Mark: 70).
- 80G-120G switch (data path only), with fair sharing and less than 10% increase in latency for all packet sizes (Mark: 80 to 90).
- 80G-120G switch, including both data path and external interfaces (Mark: 90-100).

3 Layer 1 Switch

The goal of this project is to turn the NetFPGA Layer 2 Reference Switch into a Layer 1 / Circuit switch.
Expected stages as grading:

- layer 1 switch (data path and control plane) (Mark: 60).
- layer 1 switch (data path and control plane), including hitless updates (Mark: 70).
- layer 1 switch (entire design, beyond the PCS), including hitless and consistent updates (Mark: 80 to 90).
- Same, but with a latency target of 50% of the original reference switch or better (Mark: 90-100).

4 Cut-Through Switch

The goal of this project is to turn the NetFPGA store-and-forward Reference Switch into a cut-through switch.
Expected stages as grading:

- cut-through switch (data path only) (Mark: 60).
- cut-through switch (data path only), full line rate at all packet sizes (Mark: 70).
- cut-through switch (data path and tx/rx queues), full line rate at all packet sizes (Mark: 80 to 90).
- cut-through switch (entire design), full line rate at all packet sizes (Mark: 90-100).

5 Additional Ideas

This section includes ideas for projects that need to be fleshed out by the students. It is recommended to have some prior knowledge of the base projects, as those will not be covered in class.

Low latency / High Throughput memcached server The Emu [1,2] framework, using C#, implemented a memcached server on NetFPGA. The goal of this project will be to increase the throughput / reduce the latency of the design. Such a project is likely to take the same shape as a reference switch based design (in terms of stages), but using a different design framework and application.
Additional applications available under the Emu framework include NAT and DNS.

[1] Nik Sultana, Salvator Galea, David Greaves, Marcin Wojcik, Jonny Shipton, Richard Clegg, Luo Mai, Pietro Bressana, Robert Soule, Richard Mortier, Paolo Costa, Peter Pietzuch, Jon Crowcroft, Andrew W Moore, Noa Zilberman, Emu: Rapid Prototyping of Networking Services, Usenix Annual Technical Conference (ATC), July 2017.
[2] Emu repository: `https://github.com/NaaS/emu-live/`

OSNT Enhancements OSNT [3,4] is an open source network tester running on NetFPGA. This project will attend to current performance limitations of the OSNT platform, such as the ability to capture on multiple ports at once, higher capture resolution etc.

[3] Gianni Antichi, Muhammad Shahbaz, Yilong Geng, Noa Zilberman, Adam Covington, Marc Bruyere, Nick McKeown, Nick Feamster, Bob Felderman, Michaela Blott, Andrew W. Moore, Philippe Owezarski. "OSNT: Open Source Network Tester", IEEE Network, IEEE Network, vol.28, no.5, pp.6,12, September-October 2014.
[4] OSNT website: `http://osnt.org/`