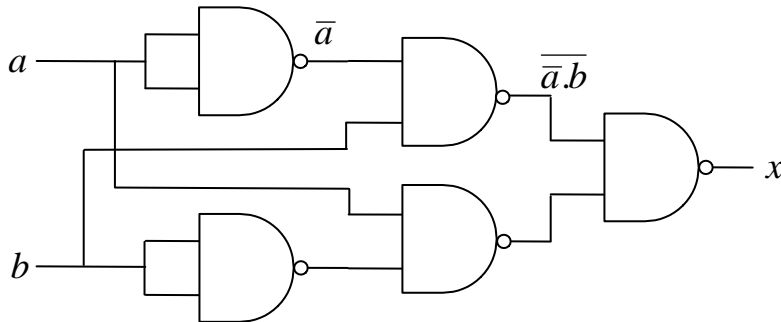


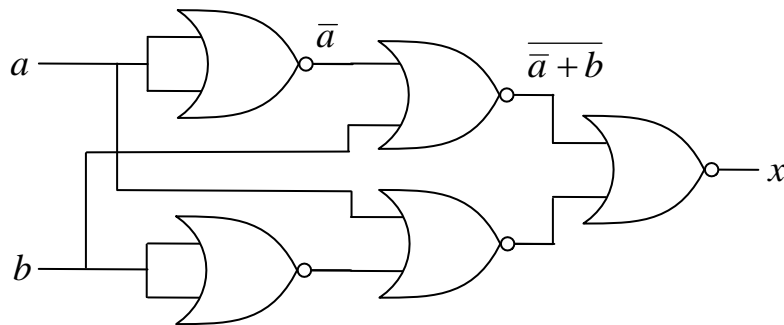
IA – Digital Electronics

Examples Paper

1. Complete the truth tables for the following digital logic circuits.



a	b	\bar{a}	$\bar{a}.b$		x
0	0				
0	1				
1	0				
1	1				



a	b	\bar{a}	$\bar{a} + b$		x
0	0				
0	1				
1	0				
1	1				

2. Use Boolean algebra to prove the following identities:

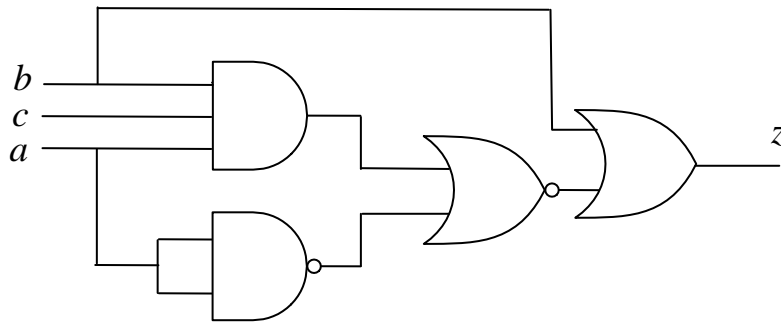
$$a.b.c + a.b.\bar{c} = a.b$$

$$a.(\bar{a} + b) = a.b$$

$$a.b + \bar{a}.c = (a + c).(\bar{a} + b)$$

$$(a + c).(a + d).(b + c).(b + d) = a.b + c.d$$

3. The following circuit does not make efficient use of logic gates. Write a Boolean expression for z , and hence show how z can be realised more efficiently.



4. A logic 'voter' circuit has 4 inputs a, b, c, d and one output v . The output is to be logic 1 if any 3 or all 4 inputs are at logic 1. Design a circuit using AND and OR gates to satisfy this requirement.

5. Devise circuits to solve question 4 if

- (a) NAND gates only;
 (b) NOR gates only are to be used.

6. Using a Karnaugh map, write simplified sum of products expressions for f and \bar{f} where,

$$f = \bar{a}.\bar{d} + \bar{b}.\bar{c} + \bar{a}.b.\bar{c}.d$$

and $a.\bar{b}.c.\bar{d}$ is a don't care state.

7. A three variable function is given by:

$$f = a.\bar{b}.\bar{c} + a.\bar{b}.c + a.b.c$$

Find the simplest sum of products form for f using a Karnaugh map. Express f using:

- (a) NAND gates only;
 (b) NOR gates only. (Hint: try mapping \bar{f} for fewest gates)

8. The function f in question 7 can be written in the form:

$$f = 100 + 101 + 111 = \sum(4,5,7)$$

Find the simplified sum of products and product of sums forms for the four variable function g where:

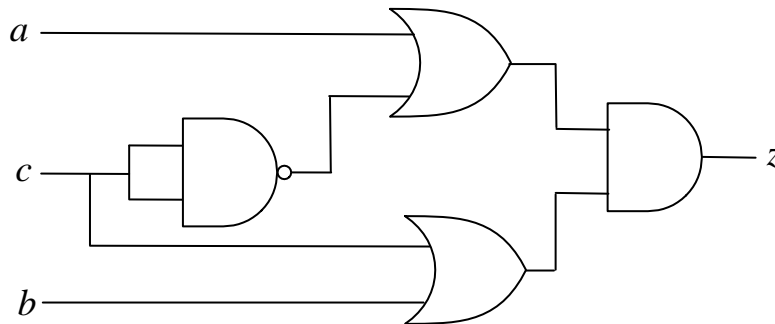
$$g = \sum(5,6,7,8)$$

and terms 10 to 15 inclusive are don't care states. Take $abcd$ to be the four variables, with a the most significant.

9. The months of the year are coded in binary with January represented by $A_3, A_2, A_1, A_0 = (0001)$ and December by (1100) . Find a simplified sum of products expression in terms of A_3, A_2, A_1, A_0 for the months without an r in their name.

Show that a simpler expression is obtained by changing the coding so January is represented by (0000) and December by (1011) .

10. Each gate in the following circuit has a propagation delay of τ .



(a) Draw a timing diagram showing the output of each gate for $a = b = 0$; and c initially 0, switching to 1 for a time t ($t \gg \tau$), and then returning to 0. Hence show that a static hazard exists. Is it a static 1 or static 0 hazard?

(b) Write down a product of sums expression for z from the circuit and use de Morgan's theorem to obtain a sum of products expression for \bar{z} .

(c) Draw a Karnaugh map for \bar{z} and thus show how the hazard can be removed by adding one more OR gate to the circuit.

11. (a) Calculate the 2's complement 8-bit signed binary representation of the decimal numbers -38 and 100 . Show that the bit pattern for -38 may be added to that for 100 effectively forming $(100-38)$, and the 'right' answer interpreted if we ignore the extra 9th bit. Convert the 8-bit binary answer to decimal and hexadecimal.

(b) Write out the following hexadecimal sequence in binary (4-bit words).

2, 6, 7, 5, 4, C, D, F, E, A

Observe that only one bit changes at each step along the sequence. Show how this unit-distance sequence can be represented as a path around a 4 by 4 Karnaugh map.

12. A logic circuit has 4 inputs and 4 outputs. The four inputs A_1, A_0 and B_1, B_0 represent two unsigned 2-bit numbers. The outputs are the four bits of the product of the input numbers.

Express the logic functions for each term P_3, P_2, P_1, P_0 in the product on a Karnaugh map of the four input variables.

Hence design a multiplier circuit using 4-input NAND and inverter gates only.

13. The input to the first stage of a five-stage shift register is obtained from the exclusive-OR function of the outputs of the 3rd and 5th stages. Consider at the start that all 5 stages have a 1 output that shifts to the right on the application of each clock pulse. What is the output sequence expressed as a decimal number, taking the right (5th) stage as the least significant bit? After how many clock pulses does it repeat?

What happens if all 5 stages have 0 set on them at the start?

14. The six states of a divide-by-six counter using 3 D-Type FFs are given in the following table and use the natural binary count. Determine the next state logic for the 3 FF inputs.

FF outputs		
C	B	A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1

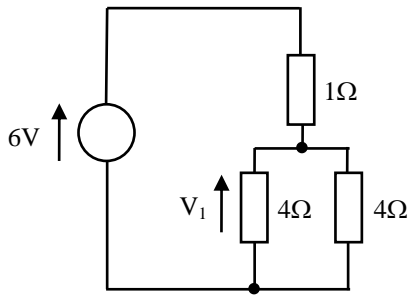
15. Design a divide-by-four synchronous counter that will count up (natural binary, i.e., 00, 01, 10, 11, etc.) when an input $Z = 0$, and that will count down (natural binary) when $Z = 1$. Use two D-type FFs.

16. Draw the state diagram only for a system with a single input Y , connected to a line carrying serial digital data on which it is desired to detect a sequence $Y = 0010$. The sequence 00100010 should give an output twice at the instants underlined.

17. Gray codes have a sequence where only one bit changes at any one time. A two-bit Gray code is 00, 01, 11, 10, 00, Design a machine using D-Type FFs to generate this Gray code sequence.

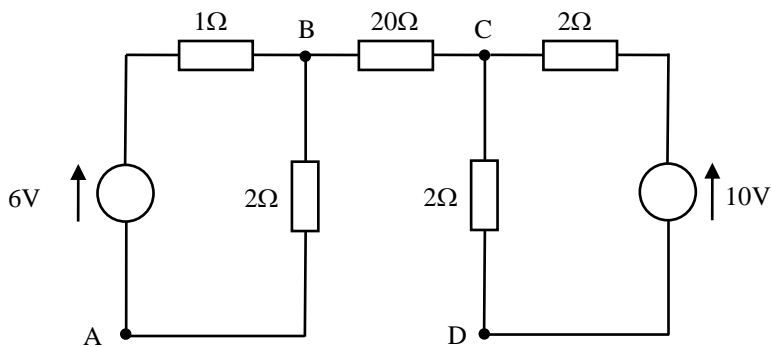
18. Use the two-bit Gray code machine you designed in question 17 as the basis for generating the traffic light sequence, Red, Red and Amber, Green, Amber, Red,

19. For the following circuit:



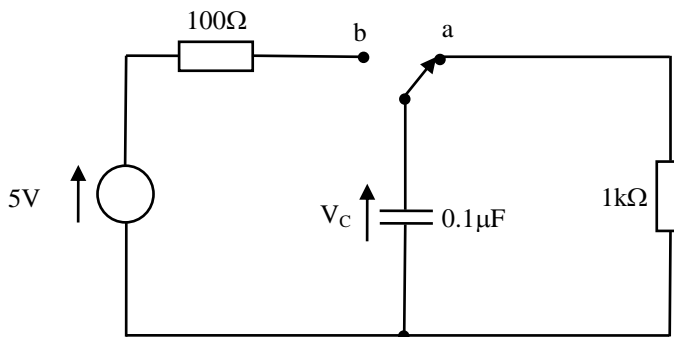
- What is the current through the 1Ω resistor?
- What is voltage V_1 ?
- What power is dissipated in each of the 4Ω resistors?

20. For the following circuit:



- What is the current flowing through the 20Ω resistor?
- Find the voltage at nodes B, C, and D with respect to node A, i.e., V_{AB} , V_{AC} and V_{AD} .

21. For the following circuit:



Initially the $0.1\mu\text{F}$ capacitor is discharged, i.e., $V_C = 0\text{V}$ and the switch is in position **a**.

At time 0s the switch is moved to position **b**.

- What is V_C at $t = 5\mu\text{s}$?
- What is the initial current flow at $t = 0\text{s}$?

At $t = 100\mu\text{s}$ the switch is moved back to position **a**.
 (c) How long does it take V_C to fall to 2.5V?

22. The n-MOS FET with the characteristics shown in Fig. 1(b) is used to implement the inverter circuit shown in Fig. 1(a).

- (a) Draw a load line (i.e., resistor characteristic) on Fig. 1(b) and determine the output voltage V_o , corresponding to input voltages V_i , of 0V and 10V.
- (b) Calculate the power dissipated in the 500Ω resistor and the transistor for each input voltage.

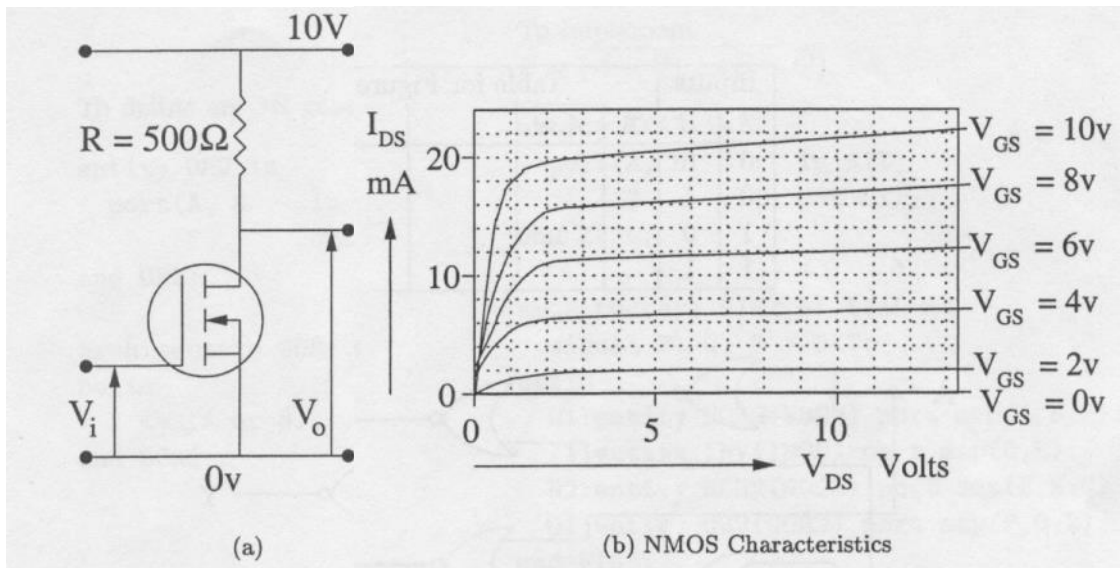


Figure 1: