SoC D/M Exercise Sheet, 2014/2015

This sheet contains exercises of various lengths. Many exercises are nominally allocated marks at Tripos examination level (i.e. with 20 marks making a full exam question).

There is some repetition of material between the exercises, so a suitable target is to solve approximately one third of them. Exercises marked with a ♡ form a recommended core. Some sections contain additional preference instructions.

Example answers are available to supervisors.

SP6a: SystemC Overview Exercises

In this section, questions are not divided into short or long, but those marked with a heart (♡) are recommended and the rest should be skimmed over.

Note: although fully covered in the RTL section from the users' perspective, internal implementation of the signal paradigm and non-blocking assignments was not lectured in SystemC or EDS in 2015.

SYSC1. Describe the principle features of SystemC. [5 Marks]

SYSC2. With what user syntax and how internally is an RTL-style non-blocking assignment achieved in SystemC ? [5 Marks]

SYSC3. How is design module heirarchy expressed in SystemC ?

SYSC4. ♡ Why adapt a general-purpose language like C++ for hardware use when special hardware languages exist ? [2 Marks]

SYSC5. ♡ To what level of detail can a gate-level design be modelled using SystemC, would one ever want to do this and what simulation performance might be achieved ? [5 Marks]

SYSC6. Give a fragment of SystemC or RTL that relies on its kernel scheduler to correctly implement non-blocking updates (avoiding shoot-through) and then give an equivalent fragment of pure C that has the same behaviour but which does not need support from a scheduler or other library. [10 Marks]

SYSC7. How does SystemC help model registers that have widths not native to the C language ? [4 Marks]

SYSC8. Give synthesisable SystemC for a five-bit synchronous counter that counts up or down dependent on an input signal. *You should sketch C++ code that looks roughly like RTL rather than worrying about a precise definition of synthesisable for SystemC.* [5 Marks]

SYSC9. Define suitable nets for a simplex interface that transfers packets of 3 bytes over an asynchronous eight-bit bus with a protocol that is based on the four phase-handshake. Describe the protocol. *Answer this part using RTL, timing diagrams or natural language.* [5 Marks]

SYSC10. Sketch SystemC RTL-like code for a synthetic data generator that creates three byte packets and delivers them over the four-phase interface of SYSC11.. *Precise syntax and operational details are unimportant, but a sensible answer would be a Verilog module that puts a counting sequence in the packet payloads.* [5 Marks]

Practical Exercise: Using the RTL-style blocks provided in the 'toy classes' with the nominal processor, please experiment with various configurations and understand how you would make a more-complex system using more of the addr_decode and busmux components to address the components.

`ssh linux.pwf.cam.ac.uk: /ux/clteach/SOCDAM/thisyears-toyclasses`

SP6b - ESL (Electronic System Level) and TLM Exercises

Please look mainly at those exercises marked with ♡ .

ESL1. ♡ Briefly explain how and why an ESL model that uses a TLM model of its busses can run the embedded software with no modification to its device drivers. [4 Marks]

ESL2. ♡ Explain how the device driver for an on-chip network might be modified if the network device itself is not to be modelled and instead transactions are to be used to directly pass packets between network nodes. In the lectures notes, this was described as a *mid-level* model: what sort of model is logically above and below it? [4+2 Marks]

ESL3. Show how a user-defined, abstract datatype can be passed along a SystemC channel by sketching several lines of code for a packet switch, router or demultiplexer. *This was lectured and illustrated in the toy classes but industrial users today would use the TLM 2.0 convenience sockets.* [7 Marks]

ESL4. Define a transaction in Computer Science. How does the ESL use of this term differ ? [5 Marks]

ESL5. What is the difference between a blocking and non-blocking transaction in terms of implementation, efficiency and callability? [6 Marks]

ESL6. ♡ Sketch SystemC code for a shim function that converts a transactional port from blocking to non-blocking, or vice versa. (*n.b. One direction is harder than the other*). [5 Marks]

ESL7. ♡ Add a simple transactional entry point to the five-bit counter RTL-counter from the SystemC exercises sheet that allows a remote client to make a five-bit, asynchronous parallel load of a value using a TLM call. [4 Marks]

ESL8. ♡ Assume TLM calling is not synthesisable, but basic RTL-style SystemC can be converted to gates. Restructure your answer of ESL7. so that the five-bit counter has a net-level parallel load and so remains synthesisable. Then illustrate how to use a transactor to provide the TLM parallel load entry point into the now-supported, net-level parallel load. (You may ignore contention with other, simultaneous net-level operations on the counter.) [7 Marks]

ESL9. Here is some simple code for a net-level data generator consisting of a behavioural model of the data generator core and a transactor that exercises the hardware-level nets:

```
void write4p(unsigned char d)             // Transactor
{
  do (wait(clk.posedge_event()) while (ack.read())
  data = d;
  req = 1;
  do (wait(clk.posedge_event()) while (!ack.read())
  req = 0;
}

unsigned char x;
while(1) instance.write4p(x++);   //And here is a client for it.
```

Sketch code for a further part of the system which is another transactor that owns its own thread and is a client for this net-level interface which makes an upcall to a user-provided function for each byte received. [4 Marks]

ESL10. ♡ What is the advantage of putting a reference-passed delay parameter in the signature of TLM calls. [3 Marks]

ESL11. Give two ways that timing annotations embedded in a transactional-level call can be synchronised with system global time ? [5 Marks]

ESL12. Sketch a templated TLM SystemC model for a basic FIFO with capacity 8 items. [8 Marks]

ESL13. Sketch code that will join two such TLM FIFOs together to make a longer FIFO. [5 Marks]

ESL14. Sketch synthesisable SystemC or RTL-like code for such a FIFO (using either a circular buffer in a RAM or else based on a multi-stage structure). *This is rather straightforward exercise, but it is useful preparation for the next one!* [5 Marks]

ESL15. Sketch code for a transactor (one of several possible) that enables interworking between the TLM and Synthesisable FIFOs of ESL12. and ESL14.. [5 Marks]

ESL16. ♡ Sketch a SystemC model of a bus bridge and say what arbitration, queuing and address translation policies it implements. *Hint: a high-level model will likely lead to the shortest answer. It can be about six lines of code per direction. Syntax details are unimportant and, as always, pseudocode is acceptable.* [8 Marks]

ESL17. Sketch a block diagram for a SoC containing at least two identical processor cores, a DRAM controller and some amount of on-chip SRAM. Mark each end of each connection with a suitable port style to be used as part of a TLM model (eg. blocking, non-blocking, initiator, target). [10 Marks]

ESL18. Roughly estimate (order of magnitude) how many workstation instructions are used when modelling each access to the DRAM. [5 Marks]

ESL19. Consider what simulation performance an ISS might give and can it ever be faster than real time ? [5 Marks]

ESL20. Describe ways that caches can be modelled in a SoC [5 Marks]

ESL21. ♡ *a)* Why might embedded firmware be cross-compiled to native code for a workstation ? [5 Marks]

b) Give two or more ways hardware device access can be modelled when firmware including device drivers is cross-compiled for the modelling platform. [5 Marks]

ESL22. What problems might arise when using high-level models of systems that use dynamic code loading and self-modifying code ? [5 Marks]

ESL23. Briefly describe each of: cycle-accurate, approximately-timed, loosely-timed, untimed. [8 Marks]

ESL24. What is the purpose and effect of the timing quantum in the loosely-timed model? [5 Marks]. Why might a transactional system exhibit different behaviour as the quantum is adjusted ? Is this useful or just bad ? [2 Marks]

ESL25. ♡ How can contention for a resource be modelled with and without actual queuing of the transactions ?

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