Workshop Five – nMOS, pMOS and CMOS Inverters

Introduction

In this workshop you will build nMOS, pMOS and CMOS inverters and then measure their characteristics.

Components

- oscilloscope
- 1a prototyping box
- connecting wire
- pair of matched nMOS (ZVN3306A) and pMOS (ZVP2106A) FETs
- 27Ω, 470Ω, 4.7kΩ resistors
- 330nF capacitor

Step 1: Characterise nMOS Inverters

Task 1: For the nMOS inverter circuit shown below with R1 = 27Ω, use the adjacent transistor characteristics to estimate V_{out} for V_{GS} = 0V, 3V, 4V and 5V. Build the circuit on the breadboard and measure V_{out} at the specified values of V_{GS} using the oscilloscope (and its voltage cursor function) and compare them with the estimated values. Make sure you properly identify which of the FET leads is the source (S), drain (D) and gate (G) before inserting it into the breadboard. Connect the potentiometer and resistor R1 as shown.
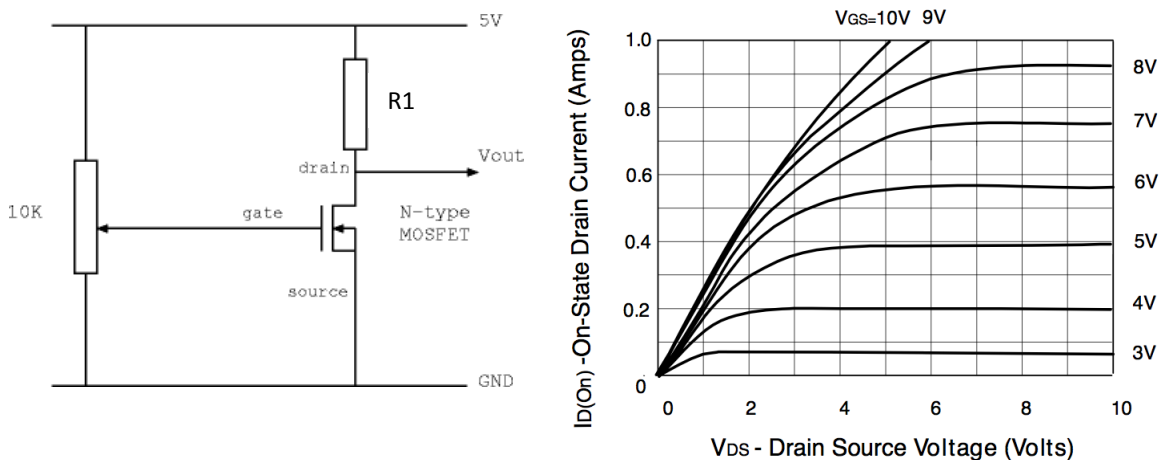
Task 2: To characterize this inverter at a more realistic value of drain current, now make R1 = 4.7kΩ. You will need to measure how the output voltage V_{out} varies with the input voltage V_{GS}. Connect one of the oscilloscope probes to the drain of the transistor and the other to the gate. Vary the gate voltage from 0 to 5V in steps of 0.2V using the potentiometer. At each step, measure the voltage at the drain. Plot a graph of drain vs gate voltage showing the transistor switching.

For the nMOS inverter, how does the current flowing through the transistor vary as the gate voltage increases?

Task 3: Find the points of negative slope (-45°) on your transfer curve. It is these points that define the boundary between valid logic levels and the indeterminate region. Using this information, find the range of valid input voltages for a logic 0 and the valid input voltages for a logic 1.

Have a look at the Appendix – Tutorial on Noise Margins, and then answer the following question. What is the noise margin of the nMOS inverter if it were connected to another similar gate?

Task 4: Investigate the effect of capacitive loading. To do this include a 330nF capacitor (C) at the output of the nMOS inverter, i.e., connect it between V_{out} and GND (OV). Disconnect the potentiometer from the input V_{GS} and instead connect V_{GS} to the Clock Generator output. Set the operating frequency to say 100Hz initially, but be prepared to change it if required later on when performing measurements of output transition times. Sketch the input and output signals observed using the oscilloscope. Specifically, for the output rising edges measure the time it takes for the signal to rise from 0V to 0.63*5V = 3.15V and compare this with the time constant CR1. Now for the output falling edges, measure the time it takes for the signal to fall from 5V to 0.37*5V = 1.85V. Why is this much shorter than the rise time? Now estimate the ON resistance of the FET.

Now make R1 = 470 Ω and repeat the previous measurements. What is the advantage and what is the disadvantage of doing this?

Step 2: Investigate pMOS Inverters

Task 1: Investigate the effect of capacitive loading. Build the pMOS inverter circuit shown below with R1 = 4.7k Ω, load capacitor C = 330nF and connect V_{in} to the Clock Generator output. Sketch the input and output signals observed using the oscilloscope and perform similar measurements to that undertaken in Step 1, Task 4 concerning the output rise and fall times. Compare this waveform with that recorded previously in Task 4, highlighting the significant differences. Calculate the theoretical waveform falling edge time (as defined in Task 4) and use the rising edge measurement to estimate the ON resistance of the pMOS FET.
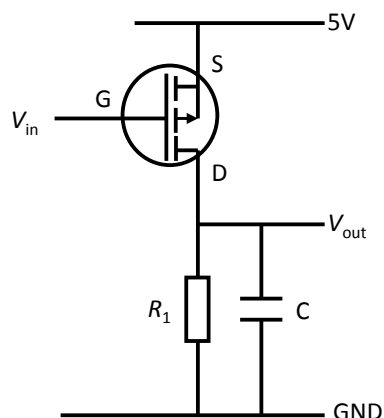

Step 3: Characterise a CMOS inverter

Task 1: The CMOS inverter circuit shown in the following figure effectively combines the nMOS and pMOS inverters shown previously. First characterise the input-output characteristic by repeating the measurement procedure in Step 1, Task 2. For the CMOS

inverter, how does the current flowing through the transistor vary as the input voltage increases?

WARNING: ensure you connect the source and drains of the transistors as shown since if you get them the wrong way around the transistors will conduct and burn out!
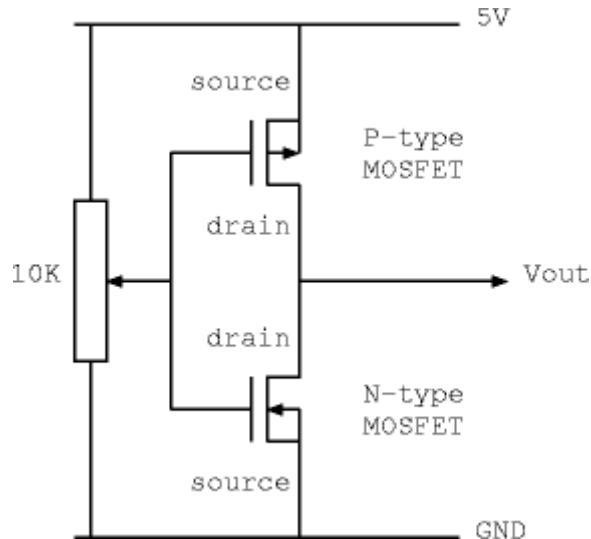
Task 2: Now investigate the noise margins as you did previously in Step1, Task 3 for the nMOS inverter. What is the noise margin of the CMOS gate if it were connected to another similar gate?

Task 3: Investigate the effect of capacitive loading. To do this add a 330nF capacitor (C) at the output, i.e., connect it between V_{out} and GND (OV). Disconnect the potentiometer from the inverter input and instead connect the inverter input to the Clock Generator output. Set the operating frequency to say 100Hz initially, but be prepared to change it if required later on when performing measurements of output transition times. Sketch the input and output signals observed using the oscilloscope. Compare this waveform with those observed previously for the nMOS and pMOS inverters and note down the significant differences. What other advantage does the CMOS inverter have over the nMOS and pMOS inverters?

Assessment

Ticking criteria: Write up your experimental data and answer the questions.

Once your work has met the Common Ticking Criteria (see Introduction), get your work ticked by an assessor. Remember that you need to hand in this assessed exercise as part of your portfolio of work (see the Head of Department's notice).

Appendix - Tutorial on Noise Margins

If you look at the electrical characteristics section of the data sheet for a 74HC series IC, you will find that the manufacturer guarantees that the gate will recognise any input voltage above 2.4V as a logic 1 and will recognise any input voltage below 2.1V as a valid logic 0 input.

On the output side of the gate, the minimum guaranteed logic 1 output voltage is given as close to VCC (in our case 5V). The maximum logic 0 voltage is around 0.1V.

Notice that the minimum output high voltage (4.9V) is 2.5V higher than the minimum voltage required for an input high on a following gate (2.4V). A difference of 2V also exists between the maximum logic 0 output voltage and the maximum logic 0 input voltage. These differences are referred to as noise margins. They ensure that a small noise transient on a connecting wire cannot change the state of the next gate. It is normal to quote the smaller of the two values; in this case our inverter has a noise margin of 2V.
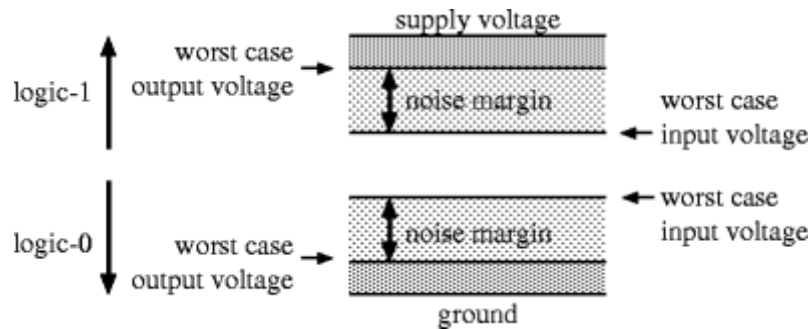
Appendix 2 – nMOS Transistor Characteristics