

Multi-terminal Nets do Change Conventional Wire Length Distribution Models

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ABSTRACT

Conventional models for estimating wire lengths in computer chips use Rent's rule to estimate the number of terminals between sets of gates. The number of interconnections then follows by taking into account that most nets are point-to-point connections. In this paper, we introduce a model for multi-terminal nets and we show that such nets have a fundamentally different influence on the wire length estimations than point-to-point nets. The multi-terminal net model is then used to estimate the wire length distribution in two cases: (i) the distribution of source-sink pairs for applications of delay estimation and (ii) the distribution of Steiner tree lengths for applications related to routing resource estimation. The effects of including multi-terminal nets in the estimations are highlighted. Experiments show that the new estimated wire length distributions are close to the measured ones.

Keywords

Wire length estimation, Multi-terminal nets, Rent's rule.

1. INTRODUCTION

Conventional length estimation models employ a model for the circuit, a model for the architecture (standard cell, gate array, etc.) and a layout model to predict wire lengths in digital designs a priori, i.e., before the actual layout has been performed. Such models are based on *Rent's rule* [7, 4] which predicts that the number of terminals T needed for communication between a module of a partitioned circuit and the remaining of the circuit is related to the number of gates B in the module as

$$T = t B^p \quad (1)$$

with t the average number of terminals per gate (if $B = 1$,

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$T = t$)¹ and p the Rent exponent. This exponent provides the necessary information on the complexity of the interconnection topology of the circuit as well as on the level of placement optimization [4].

Wire length estimates based on Rent's rule were introduced by Donath [6] in 1979 and are getting more attention recently. Several improvements have been presented [13, 5, 8, 14, 11]. An overview of wire length estimation methods is presented in [4]. These methods all estimate the number of terminals needed for communication between two sets of gates from Rent's rule, predict the number of nets from the number of terminals and estimate the average length of each of those nets. The prediction of the number of nets from the number of terminals is generally done by assuming only point-to-point (i.e., two-terminal) nets. While it is acknowledged that multi-terminal nets exist, it is assumed that the number of point-to-point nets is significant enough to dominate the wire length distribution.

Multi-terminal nets have been studied in [12, 18]. Both papers suggest a model for multi-terminal nets and compute from that the distribution of nets over their number of terminals. We will call this the *net degree distribution*. The predicted distributions are then validated by comparing them to the measured net degree distribution. In this paper, we investigate the influence of the multi-terminal nets on the wire length distributions by considering two application models for the wire length estimations. A first application model uses the wire delay. For such *delay-related applications*, the length of connections between a source and a sink is important. The length of other branches in the net (from sinks to other sinks) is only of secondary importance. A second application domain is situated in the field of estimating routing resources. For such *routing-related applications*, the entire Steiner tree length of nets is the only length that counts. We will show that both application domains result in a different solution to the wire length estimation problem. Moreover, the solutions are fundamentally different from the point-to-point solution found in all previous works.

Section 2 briefly reviews the multi-terminal net model from [12] and [8], focusing on those aspects of the model that are used for the multi-terminal net length estimations of section 3. In that section, a wire length prediction model is proposed for both delay-related and routing-related applications. The resulting wire length distributions and average wire lengths are then compared to experimentally measured lengths in section 4.

¹This is only approximately true since t is generally found by fitting a logarithmic curve to a terminal-versus-gate plot.

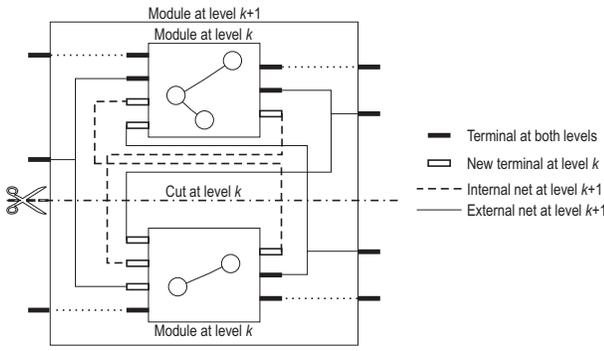


Figure 1: The difference between cutting internal nets (dashed lines) and external nets (solid lines).

2. MODEL FOR MULTI-TERMINAL NETS

2.1 The number of (multi-terminal) nets

Consider a recursive four-way² partitioning of a circuit, minimizing the number of terminals. Rent's rule (equation 1) can then be applied to the partitioning modules and provides an estimate for their average number of terminals. Suppose the circuit contains a total of $G = 4^K$ gates, recursively divided into 4 modules of (equal) size $B = 4^k$ at each partitioning level k ($k = 0$ at the lowest level where each module contains only a single gate and $k = K - 1$ for the partitioning of the entire circuit into 4 modules). The total number of terminals for all modules of size B then is

$$T_{tot}(B) = t B^p \frac{G}{B} = t G B^{p-1} \quad (2)$$

and the number of terminals T_k that is generated by the cutting of nets at hierarchical level k by

$$T_k = T_{tot}(4^k) - T_{tot}(4^{k+1}) = t G 4^{k(p-1)} (1 - 4^{p-1}). \quad (3)$$

Previous wire length estimation models simply relate the number of terminals T_k at level k to the number of nets N_k cut at level k by assuming point-to-point nets only, hence $N_k = \frac{1}{2} T_k$. In the best case, they account for multi-terminal nets by introducing a factor α ($1/2 \leq \alpha \leq 1$) instead of $1/2$ [6]. However, the relation between N_k and T_k is more complicated in the case of multi-terminal nets [12, 8, 11].

Consider the partitioning process at level k (figure 1). An *internal net at level k* is entirely contained in one module of the partitioning level k . An *external net at level k* has a terminal at level k . During partitioning, both internal and external nets can be cut. Cutting an internal net generates two new terminals (figure 1). An external net at level $k + 1$, on the other hand, already uses a terminal at level $k + 1$ so only one new terminal has to be generated (the other one can be reused). With $S_{i,k}$ the total number of internal nets cut at level k and $S_{e,k}$ the total number of external nets cut at level k , this implies³

$$2 S_{i,k} + S_{e,k} = T_k. \quad (4)$$

²The reasoning is also valid for another partitioning but a four-way partitioning is beneficial for the model in section 3.

³There exists an important difference between the often used cut minimization partitioning criterion and the terminal minimization criterion. Indeed, equation 4 indicates that cutting internal nets is much more disadvantageous, in terms of the number of new terminals generated, than cutting external nets. A detailed analysis is presented in [9].

The new terminals created by the cutting of nets can be input or output terminals. We define γ_k as the ratio of the number of new output terminals to the total number of new terminals

$$\gamma_k = \frac{O_k}{T_k}. \quad (5)$$

Due to the self-similarity of circuits at different hierarchical levels, it is acceptable to assume that γ_k is independent of the hierarchical level k [8, 11], i.e., $\forall k : \gamma_k = \gamma$. Figure 1 shows that the total number of nets cut at level k equals the number of new input terminals, i.e., $(1 - \gamma) T_k$. The parameter γ can be found from the total number of internal nets in the circuit (i.e., the total number of nets N minus the number of external nets, or pins, P) as [11]

$$\gamma = \frac{N - P}{tG - P} = \frac{G t_o - O}{tG - P}. \quad (6)$$

The last part of equation 6 is found by using a relation between N and the number of primary inputs (I) and outputs (O) of the circuit and the average number of inputs (t_i) and outputs (t_o) per gate. Since nets can only be driven by gate outputs or primary input pins and since each net is driven exactly once, $N = G t_o + I$. Equation 6 results in $\gamma \leq 1/2$:

$$\gamma \leq \frac{1}{2} \Leftrightarrow 2N - 2P \leq tG - P \Leftrightarrow \frac{tG + P}{N} \geq 2. \quad (7)$$

Indeed, the ratio of the total number of terminals over the total number of nets, i.e., the average net degree (we count external terminals in the net degree), is always larger than (or equal to) 2.

From the above, we can calculate the total number of internal ($N_{i,k}$) and external nets ($N_{e,k}$) at a hierarchical level k , as well as the number of internal ($S_{i,k}$) and external nets ($S_{e,k}$) that is cut at level k (see [11] for the exact equations).

2.2 Net Degree Distributions

The previous section calculates the number of internal and external nets at each recursion level. In this section, we seek to identify the net degree of each of these nets, i.e., the net degree distribution. We benefit from using its moment generating function, which we will call the *generating polynomial for net degrees* [15]. It is a polynomial in the variable x for which the coefficients of each term x^n are given by the number d_n of nets with net degree $\nu = n$ and it is denoted as $\mathcal{V}_n = \sum_n d_n x^n$. The normalized version is called \mathcal{W}_n .

In [12, 8, 11], a recursive equation is found for the net degree generating polynomials by using the reverse of the partitioning process, i.e., a *net generating process*. Not counting the external terminal (for this, we change the notation of $\mathcal{W}_{n,e}$ to $\mathcal{W}'_{n,e} = \mathcal{W}_{n,e}/x$), we find [12, 8, 11]

$$\mathcal{W}'_{n,e}(k+1) = g_e (\mathcal{W}'_{n,e}(k))^2 + (1-g_e) \mathcal{W}'_{n,e}(k) \quad (8)$$

$$\mathcal{V}_{n,i}(k+1) = g_i 4^{k(p-1)} (\mathcal{W}'_{n,e}(k))^2 + \mathcal{V}_{n,i}(k) \quad (9)$$

with $k \geq 0$ and

$$\begin{aligned} g_e &= (1 - 2\gamma) (4^{1-p} - 1) & \mathcal{V}_{n,i}(0) &= 0 \\ g_i &= \gamma t G (1 - 4^{p-1}) & \mathcal{W}'_{n,e}(0) &= x. \end{aligned} \quad (10)$$

Note that, if $\gamma = 1/2$, then $g_e = 0$ and the normalized net degree distribution for external nets remains the same for all levels, i.e., all external nets are two-terminal nets (counting the external terminal). By consequence, all internal nets are also two-terminal nets (equation 9).

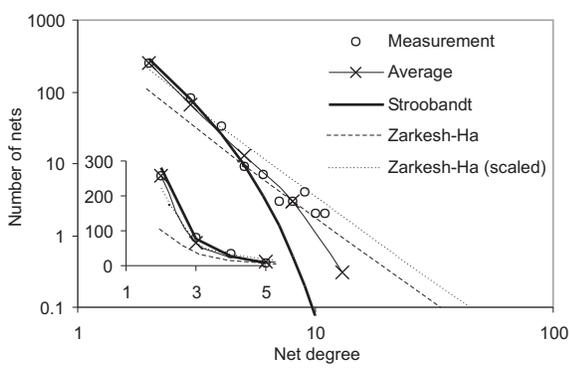


Figure 2: The measured and theoretically predicted net degree distributions for the ISCAS89 benchmark ‘s953’ in a log-log plot (inset: part of linear plot).

2.3 Average Net Degree

Although we are not able to compute closed-form expressions from equations 8 and 9, we can easily calculate the average net degree at each hierarchical level. The details of the calculation are presented in [8, 11]. The resulting average external ($\bar{\nu}_{e,k}$), internal ($\bar{\nu}_{i,k}$), and total ($\bar{\nu}_k$) net degrees at level k are found to be

$$\bar{\nu}_{e,k} = 1 + (2\gamma + (1 - 2\gamma) 4^{1-p})^k \quad (11)$$

$$\bar{\nu}_{i,k} = \frac{(2\gamma 4^{p-1} + 1 - 2\gamma)^k - 1}{\gamma (4^k (p-1) - 1)} \quad (12)$$

$$\bar{\nu}_k = \frac{N_{i,k} \bar{\nu}_{i,k} + N_{e,k} \bar{\nu}_{e,k}}{N_{i,k} + N_{e,k}} = \frac{4^k (p-1) + 1}{\gamma + (1 - \gamma) 4^k (p-1)}. \quad (13)$$

Again, $\gamma = 1/2$ leads to two-terminal nets only.

Using equation 6 for γ , we obtain the correct average net degree for the entire circuit ($k = K$ and $G = 4^K$)

$$\bar{\nu}_K = \frac{tG + tG^p}{N}. \quad (14)$$

Both the average net degree of internal nets (equation 12) as the one for all nets (equation 13) approach $1/\gamma$ for very large circuits

$$\bar{\nu}_{i,k} \stackrel{k \rightarrow \infty}{\approx} 1/\gamma \quad \bar{\nu}_k \stackrel{k \rightarrow \infty}{\approx} 1/\gamma. \quad (15)$$

Based on equations 15, we can conclude that two large circuits that are different but that have the same fraction γ , produce approximately the same average net degree, independent of their respective Rent exponents! This means that the fraction γ is a separate circuit property and an extra parameter, next to the Rent exponent.

2.4 Net Degree Distribution Evaluation

To validate the recursive equation for the net degree distribution, we compare it to measurements on the ISCAS89 benchmark ‘s953’ [2] and the benchmark ‘industry3’ [1] (see figures 2 and 3). The Rent exponent has been estimated by fitting a straight line to the data generated by the partitioning program ‘ratiocut’ [16]. The output fraction γ is found from equation 6 and from the measurements of N and P from the benchmark data. Figures 2 and 3 show that the measured net degree distribution for internal nets and the theoretically predicted distribution follow the same trend as a function of the net degree n (compare with the

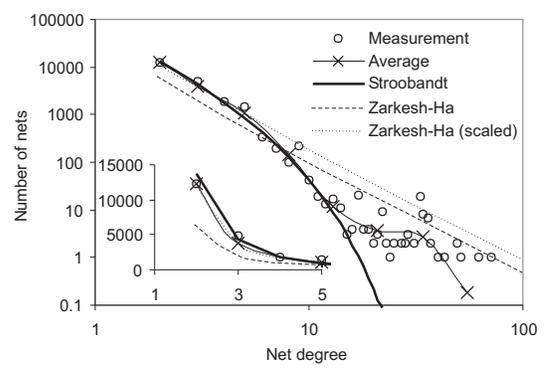


Figure 3: The measured and theoretically predicted net degree distributions for the benchmark ‘industry3’ in a log-log plot (inset: part of linear plot).

curve of average values). The correlation between both distributions is very good for the small net degrees (largest number of nets). The net degree distribution found by Payman Zarkesh-Ha [18] is also shown in the figures as a dashed line, with the same parameters as in our model (measured from a circuit partitioning). While our model only underestimates the number of nets with very high net degree,⁴ the model found by Zarkesh-Ha largely underestimates the total number of nets (by a factor ≈ 2). Even if we scale the model to the total number of nets, it underestimates the nets with few terminals and largely overestimates the number of nets with a lot of terminals. Our model predicts the net degree distribution more accurately. There are several reasons for this. In [18], the authors only consider multi-terminal internal nets (no external nets) when calculating the number of nets from the number of terminals (and thus they implicitly assume $\gamma = 1/2$). In their recursive calculation model, they also assume that, for the addition of one gate to a module of B gates, all additional nets are $(B+1)$ -terminal nets whereas it is clear some (or even most) of the new internal nets will have a lower number of terminals (i.e., they do not have to be connected to all gates of the modules). Also, unlike the Zarkesh-Ha model, our model finds the exact average net degree (equation 14).

3. WIRE LENGTH ESTIMATION FOR MULTI-TERMINAL NETS

Ever since Donath introduced his wire length estimation method at the end of the 70’s [6], it has been used by nearly every researcher engaged in a priori wire length estimation. In Donath’s method, the circuit is basically characterized by the complexity of its interconnection topology, described by Rent’s rule and the Rent exponent. The Manhattan grid serves as a model for the physical architecture the circuit will be placed in and the placement process itself is modelled by a theoretical placement minimizing the total wire length (i.e., the sum of all distances between connected gates). Since it is assumed wires are always routed along the shortest path, the wire length follows from the placement information alone.

⁴Note that the actual number of nets with high net degree no longer follows the average behaviour and that these nets are probably special nets. Also, the number of such nets is negligible compared to the total number of nets.

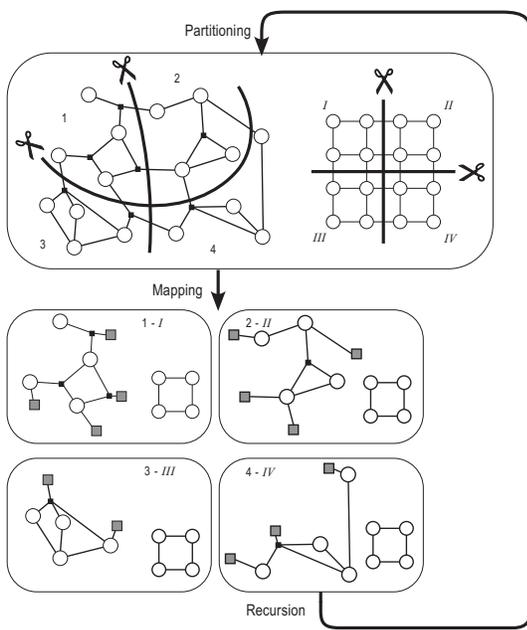


Figure 4: Donath's hierarchical partitioning of the circuit and the physical architecture.

3.1 Donath's Hierarchical Placement Model

Donath's placement model is summarized in figure 4. The circuit is partitioned into four subcircuits of equal size (denoted by 1, 2, 3, and 4), in such a way that the partition satisfies Rent's rule [7]. The square Manhattan grid is also partitioned into four subsquares of equal size, in a symmetrical way (denoted by I, II, III, and IV) and each subcircuit is mapped to a subsquare. This process is then repeated recursively for each of the subcircuit subsquare pairs, until all gates are assigned to exactly one grid cell. Compared to the random placements one used before, Donath's hierarchical placement models placement optimization better. It is also easily combined with our multi-terminal net model.

All interconnections are assigned to a particular level of hierarchy in the placement process and the average number of interconnections N_k at level k is calculated (from Rent's rule), as well as the average wire length per level $\bar{\ell}_k$. The average wire length $\bar{\ell}$, computed over all hierarchical levels, is then given by

$$\bar{\ell} = \frac{\sum_{k=0}^{K-1} N_k \bar{\ell}_k}{\sum_{k=0}^{K-1} N_k}. \quad (16)$$

With this, we can focus the discussion on the average wire length $\bar{\ell}_k$ per level and the number of wires N_k at each level.

3.2 Average Wire Length per Level

For the average wire length $\bar{\ell}_k$ of a connection assigned to level k , we use an extension of Donath's technique that takes placement optimization better into account. We therefore write the wire length distribution $\mathcal{D}_{\ell,k}$ at a hierarchical level k as the product of a *structural distribution* $S_k(\ell)$ and an *occupation probability* $q(\ell)$ [4, 5, 14]

$$\mathcal{D}_{\ell,k} = S_k(\ell) q(\ell). \quad (17)$$

The structural distribution is the enumeration of all possible

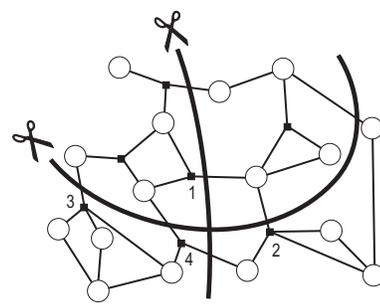


Figure 5: Hierarchical four-way partitioning of the circuit. Net 4 is split into more than two parts.

paths in the architecture at the hierarchical level.⁵ It represents the entire collection of placement sites for nets at the hierarchical level. The occupation probability then assigns to each of the placement sites a probability that the site is occupied by a wire at hierarchical level k [14, 8]. The occupation probability $q(\ell)$ can be approximated by ℓ^{2p-4} for a two-dimensional Manhattan grid [4, 5, 14]. The expected value of the average length of wires at hierarchical level k then equals

$$\bar{\ell}_k = \frac{\sum_{\ell=0}^{\ell_{max}(k)} \ell S_k(\ell) q(\ell)}{\sum_{\ell=0}^{\ell_{max}(k)} S_k(\ell) q(\ell)} = \frac{\sum_{\ell=0}^{\ell_{max}(k)} S_k(\ell) \ell^{2p-3}}{\sum_{\ell=0}^{\ell_{max}(k)} S_k(\ell) \ell^{2p-4}}. \quad (18)$$

In [8, 14] it is shown that the wire length (over all hierarchical levels) scales with ℓ^{2p-3} .

3.3 Average Number of Interconnections

In section 2 we found that the number of nets at level k is related to the number of terminals as $N_k = (1 - \gamma)T_k$. In practice, older methods are equivalent to splitting each multi-terminal net into a number of net segments that can be calculated separately in the length computation as two-terminal nets. Note, however, that the computed length then is not the total net length but the net segment length. We will extend previous methods to realistic net lengths by recombining these net segments.

A first problem we have to note is the different hierarchical partitioning structures between a bi-partitioning and a four-way partitioning. Consider the four-way partitioning of figure 5. The multi-terminal nets 1, 2 and 3 are split into two parts as in the bi-partitioning scheme. These nets will still generate one or two new terminals depending on whether they are external or internal. However, net 4 is split into three parts and hence generates three new terminals (as an internal net). This complicates the analysis of the multi-terminal net model since only the total number of internal and external nets can be computed but not the fraction of that number that is kept in two modules and the fraction that uses more modules. This fraction is likely to depend on the net degree distribution. On the other hand, a good partitioning and placement strategy will try to keep connected gates close to each other and therefore it will reduce

⁵See [15] for an efficient way to enumerate the distributions using generating polynomials.

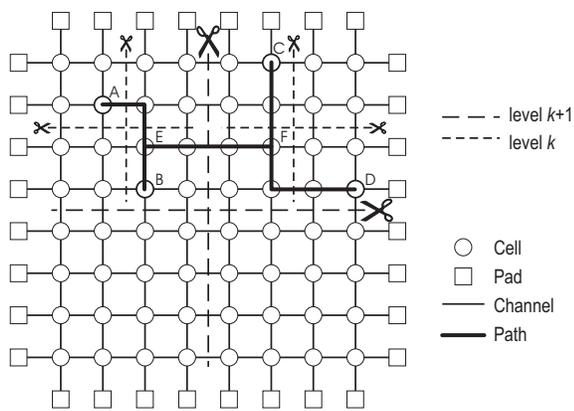


Figure 6: The decomposition of a multi-terminal net (Steiner tree) into net components over several hierarchical levels: difference between delay-related and routing-related applications.

the possibility of splitting a net into more than two modules (also note that the increase in number of terminals would be punished in the partitioning cost function). For these reasons, we assume that nets are only split into two parts in a four-way partitioning process. With this assumption, we can directly reuse all results from section 2.

As explained in the introduction, there are two ways in which we should account for multi-terminal nets in length calculations. For delay-related applications, we split each n -terminal net into $n - 1$ point-to-point source-sink pairs. For routing-related applications the total length of the multi-terminal net will be computed as the sum of lengths of its net segments. In both cases, we simplify the length estimation by splitting up multi-terminal nets into 2-terminal components. However, both cases differ fundamentally in the number of nets that are assigned to each hierarchical level and in the length of these nets. We do not change the length calculation from section 3.2 but we change the number of net (segments) considered at each level as well as the way in which their lengths are combined.

3.3.1 Delay-related Applications

A source-sink pair is counted at hierarchical level k if the path between source and sink is cut at that level. Consider the multi-terminal net in figure 6 and assume, without loss of generality, that gate A is its source. According to our convention, the path A-B will be at hierarchical level k , the paths A-C and A-D at level $k + 1$. So, the number of source-sink pairs at level $k + 1$ equals the number of net segments cut at that level times the average number of sinks in the module not containing the source of the nets. Both quantities are known from the multi-terminal net model of section 2. The net in figure 6 counts for two source-sink pairs (A-C and A-D) at level $k + 1$ although only one net segment is cut (E-F). The same rule assigns one source-sink pair (A-B) to level k . Note that also the net segment (C-D) is cut at level k but that it is not counted as a source-sink pair because the source is in none of the two modules at that level. The details of the calculations can be found in [11, 10].

A numerical evaluation of the number of source-sink pairs for a circuit with Rent exponent 0.6, placed in a Manhattan grid of 1024 by 1024 cells, with an average number of

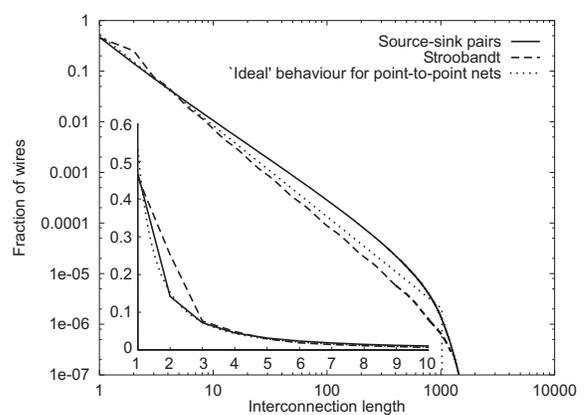


Figure 7: Comparison of the new source-sink length distribution with Stroobandt's distribution [14, 8] and the scaling behaviour l^{2p-3} (normalized on [1..1024]) ($G = 4^{10}$, $p = 0.6$; inset: part of linear plot).

input terminals per gate of 3 (1 output) and 20% of the pins that are primary outputs, results in the wire length distribution plotted in figure 7. The length distribution for source-sink pairs is not too far away from the old length distribution. This is due to the fact that the older distributions estimated lengths for net segments, which is not too distinct from estimating source-sink pairs as in our new method. Especially for short wire lengths, the new distribution is quite close to Stroobandt's and to the expected scaling behaviour for point-to-point nets. However, the length distribution of source-sink pairs has a slightly different scaling behaviour than the older model and the "ideal" behaviour for point-to-point nets. This is because the number of source-sink pairs has the same scaling behaviour as previously only if $\gamma = 1/2$, i.e., for two-terminal nets only. For multi-terminal nets, some net segments are counted for several source-sink pairs and therefore the source-sink pair distribution is situated above the older one, especially for higher lengths. This illustrates the importance of including multi-terminal nets in the estimations.

3.3.2 Routing-related Applications

For routing-related applications we split the Steiner net into several *net segments* between two gates, between a gate and a Steiner point, or between two Steiner points. The segments are defined by the (four-way) partitioning scheme and assigned the level on which they are cut. Figure 6 shows the principle behind this: the segments A-B and C-D of the four-terminal net are cut on level k and these two net segments are connected at level $k + 1$ by a net segment between the Steiner points E and F. Each of the net segments is considered as a two-terminal net but to find the total Steiner tree length we have to add lengths of net segments (of different levels) belonging together. The calculation of the overall Steiner length distribution uses the same generating polynomials as in equations 8 and 9 and is detailed in [11, 10].

The combination of the lengths of net segments will naturally result in a wire length distribution with longer wires than in the case of source-sink pairs. A numerical evaluation in figure 8 confirms this. Naturally, the estimate of the longest wires, as well as the average value, will significantly differ from the same value for the source-sink pair length.

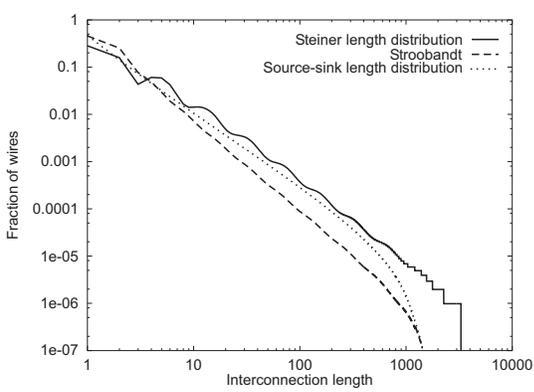


Figure 8: Wire length distribution for the entire Steiner length of multi-terminal nets, compared to the source-sink pair length distribution and the older wire length distribution model.

4. DISCUSSION AND RESULTS

4.1 Average Wire Length

For two-terminal net segments the sum over all hierarchical levels (equation 16) yields [8]

$$\bar{l} = R(p) \frac{H(K, p, 1)}{H(K, p, 2)}, \quad (19)$$

with $R(p)$ a function only depending on p and

$$H(K, p, x) = \frac{2^{K(2p-x)} - 1}{2^{2p-x} - 1}.$$

For the average source-sink pairs length \bar{l}_{ss} , it gives [11, 10]

$$\bar{l}_{ss} = R(p) \frac{2\gamma(1-\gamma)4^{p-1}G(2) + (1-2\gamma)(\gamma(1)-\gamma)G(2 \cdot 4^{1-p})}{2\gamma(1-\gamma)4^{p-1}G(1) + (1-2\gamma)(\gamma(1)-\gamma)G(4^{1-p})} \quad (20)$$

with

$$G(x) = \frac{(x(1-2\gamma+2\gamma 4^{p-1}))^K - 1}{x(1-2\gamma+2\gamma 4^{p-1}) - 1}. \quad (21)$$

The second terms in numerator and denominator of equation 20 are very small (thus reducing equation 20 to $\bar{l}_{ss} = R(p)G(2)/G(1)$), especially for large circuits, since

$$\gamma = \frac{G t_o - O}{G t - P} \approx \frac{t_o}{t} = \gamma(1) \quad (22)$$

For $\gamma = 1/2$ (two-terminal nets), equation 20 reduces to equation 19. In general however, the scaling behaviour can deviate significantly from equation 19, as shown in figure 9.

To calculate the average Steiner tree length \bar{l}_{st} , we do not need to consider the complex addition of segment lengths to Steiner lengths. The average length is simply found by dividing the total length (sum of all the individual segment lengths) by the total number of nets. This results in [11, 10]

$$\bar{l}_{st} = R(p) \frac{1-\gamma}{\gamma} \frac{H(K, p, 1)}{H(K, p, 2)}. \quad (23)$$

For $\gamma = 1/2$ (two-terminal nets), the average length is of course equal to the average net segment length (equation 19), but it is significantly higher (by a factor of $(1-\gamma)/\gamma \geq 1$) for general multi-terminal nets. Interestingly, the scaling behaviour (last factor of equation 23) is exactly the same as for segment lengths!

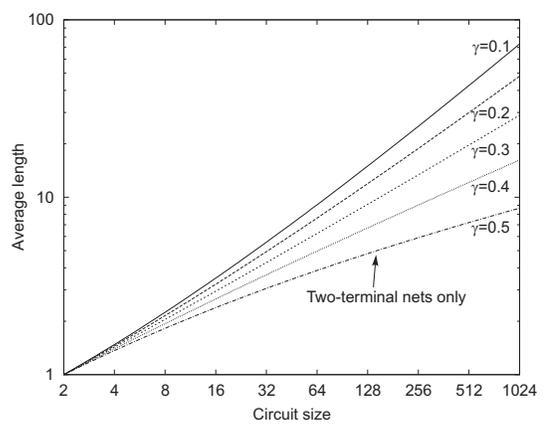


Figure 9: The scaling behaviour of the average source-sink length for different values of γ , as a function of circuit size. It is assumed that $\gamma(1) = \gamma$.

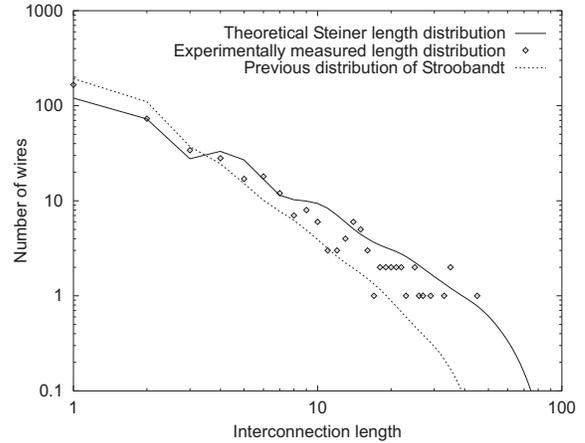


Figure 10: Comparison between the new theoretical Steiner length distribution and the real one for a placement of the ISCAS89 benchmark ‘s953’. Also shown is the previous theoretical distribution.

4.2 Experimental Verification

We compare the wire length distributions and average wire lengths from our new multi-terminal net model with experimental measurements for both source-sink pairs and Steiner tree lengths. The experimental results are obtained through placements by an in-house program based on Simulated Annealing [8]. The placement is optimized for minimal total wire length. Steiner lengths are measured using Geosteiner [17]. Because we do not have the information on which terminals are sources and which ones are sinks for our benchmark circuits, we measured source-sink lengths by taking every terminal of a net as the source ones and then averaging over the number of terminals.

The new source-sink length distributions are not too distinct from the results of the older models but for the Steiner tree lengths there is a clear difference between the new and the old models, as can be seen from figure 10. The measured Steiner lengths for the benchmark are generally longer than predicted by the older model (hence there are less short wires and more long ones) because actual Steiner lengths

Table 1: Average wire length for a placement of the ISCAS benchmark circuits. Comparison between our new estimates \bar{l} and the experimental values \bar{l}_e for source-sink pairs (subscript ss) and Steiner lengths (subscript st). The estimation error e , relative to the experimental values, is presented in %.

Name	G	p	γ	Rent								
				$\bar{l}_{e,ss}$	\bar{l}_{ss}	e_{ss}	$\bar{l}_{e,st}$	\bar{l}_{st}	e_{st}			
c432	160	0.62	0.338	3.10	2.08	-33	3.67	3.13	-15			
c499	202	0.62	0.316	3.35	1.84	-45	3.95	3.79	-4			
c880	383	0.62	0.348	2.36	2.17	-8	2.54	3.49	37			
c1355	546	0.73	0.334	2.47	2.58	4	2.87	5.24	83			
c1908	880	0.72	0.369	2.56	2.87	12	3.09	4.65	51			
c2670	1193	0.73	0.370	2.58	3.32	28	3.17	4.66	47			
c432nr	157	0.62	0.341	3.01	2.08	-31	3.56	3.09	-13			
c499nr	202	0.65	0.284	3.25	1.89	-42	3.85	3.92	2			
c1355nr	546	0.74	0.322	2.46	2.61	6	2.85	5.33	87			
c1908nr	878	0.71	0.369	2.56	2.82	10	3.09	4.49	45			
c2670nr	961	0.79	0.377	2.31	3.73	62	2.79	4.86	74			
s27	13	0.26	0.414	1.29	1.34	4	1.50	1.58	5			
s208.1	112	0.35	0.383	1.76	1.46	-17	2.08	2.04	-2			
s298	133	0.37	0.332	2.56	1.34	-48	3.26	2.72	-17			
s386	165	0.51	0.314	3.68	1.58	-57	4.03	3.44	-14			
s344	175	0.40	0.373	1.99	1.43	-28	2.14	2.27	6			
s349	176	0.40	0.371	1.98	1.44	-28	2.11	2.31	9			
s382	179	0.35	0.348	2.46	1.38	-44	2.97	2.50	-16			
s444	202	0.29	0.346	2.44	1.35	-45	2.95	2.40	-19			
s526	214	0.47	0.310	2.91	1.55	-47	3.95	3.54	-10			
s526n	215	0.43	0.311	2.90	1.51	-48	3.94	3.31	-16			
s510	217	0.65	0.338	3.93	2.12	-46	4.89	3.45	-30			
s420.1	234	0.37	0.380	1.88	1.55	-17	2.23	2.19	-1			
s832	292	0.51	0.265	6.11	1.77	-71	6.11	4.51	-26			
s820	294	0.54	0.270	5.95	1.81	-70	6.06	4.64	-23			
s641	398	0.69	0.417	2.00	2.28	14	2.10	2.96	41			
s713	412	0.71	0.404	2.02	2.40	19	2.18	3.27	50			
s953	424	0.68	0.346	3.84	2.15	-44	4.70	4.59	-2			
s838.1	478	0.41	0.378	1.95	1.68	-14	2.34	2.35	1			
s1238	526	0.66	0.329	4.40	2.29	-48	4.57	4.68	2			
s1196	547	0.64	0.345	4.11	2.24	-46	4.13	4.13	-0			
s1494	653	0.58	0.313	7.80	2.12	-73	6.89	4.52	-34			
s1488	659	0.59	0.316	7.79	2.14	-72	6.81	4.57	-33			
s1423	731	0.50	0.373	2.76	1.93	-30	2.95	2.71	-8			

are combinations of net segments. This is reflected in the new Steiner length distribution more accurately.

The results for the average wire lengths are shown in table 1 for the ISCAS85 [3] and ISCAS89 [2] benchmark circuits. These results are also shown in figures 11 and 12 for source-sink pairs and Steiner trees, as a function of the Rent exponent. In these figures, we connected the corresponding points for clarity. The rough path of the curves is due to the strong dependency of the average length on both the number of gates and the Rent exponent. Only one of these dependencies is shown in the figures.

In table 1, we can observe that (i) source-sink lengths are generally underestimated and (ii) our estimates for Steiner tree lengths are relatively close to the measured results.

The fact that actual source-sink lengths are generally a lot higher than the predicted lengths is mainly due to the optimization criterion in our experimental placement. The Simulated Annealing placement optimizes for total net length,

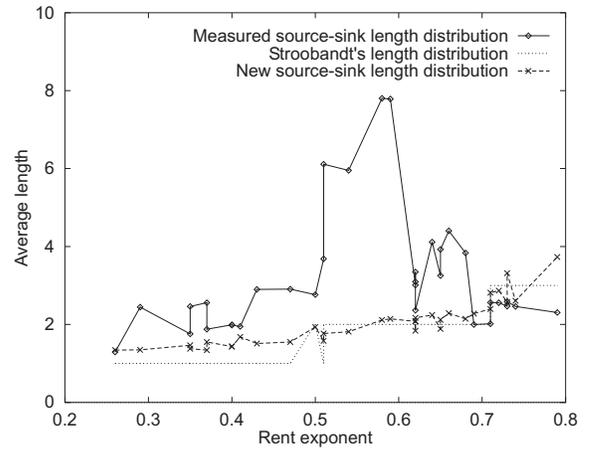


Figure 11: Comparison of our new estimates for source-sink pairs to Stroobandt's old estimates and to the experiments for the ISCAS benchmarks.

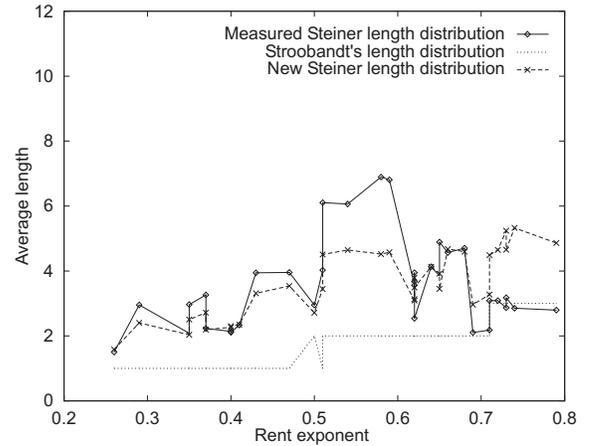


Figure 12: Comparison of our new estimates for Steiner tree lengths to Stroobandt's old estimates and to the experiments for the ISCAS benchmarks.

not for total source-sink pair length. If the program would have optimized the source-sink pair lengths it would succeed in placing the source closer to *all* of its sinks whereas it would pay less attention to the relative distances between sinks. Figure 11 also shows this and adds the older net segment estimates. The difference between the new estimates and the old estimate of Stroobandt is small because of the large similarities between estimating net segment lengths and source-sink pair lengths. However, figure 11 shows that there is some improvement in the estimates for circuits with a low Rent exponent ($p < 0.5$). For such circuits, the placement optimization is a lot easier, wires are generally very short and the effect of the optimization of the total net length instead of the source-sink lengths is smaller.

The Steiner tree estimates are much better and are within 25% of the measured values on average. However, in quite a few cases, we also underestimate this length. This is partly due to the fact that the occupation probability underestimates the number of long wires at the higher levels. For circuits that are large enough, this has no real influence on

the average wire length because the number of long interconnections is relatively small. For smaller circuits (and most of the ISCAS benchmarks are rather small), this influence is not negligible anymore. Figure 12 shows that our new model can capture the fluctuations in Steiner tree length as observed in the experimental measurements.

5. CONCLUSION

Conventional wire length estimation models do not properly take multi-terminal nets into account. In this paper, we found that there is a fundamental difference between internal and external multi-terminal nets: in a partition, the first type of nets results in two new terminals, the second one in only one new terminal. This difference is not present in analyses that only consider point-to-point connections and it leads to an exact (on average) relation between the number of new terminals generated in a hierarchical partitioning scheme and the number of nets that are cut by it. This relation also gives physical meaning to the factor α that Donath (and other researchers) introduced to “account” for multi-terminal nets.

Based on a “net generation process” described in [8, 12], we found a recursive equation for the net degree distribution which we used in this paper to estimate wire lengths for multi-terminal nets. We distinguish between “delay-related applications” and “routing-related applications.” The first type is meant for estimating delays and requires the length of source-sink pairs, the second type is related to routing resources and considers Steiner tree lengths. We presented a wire length estimation technique for both source-sink pairs and Steiner tree lengths that uses the best-known previous models for estimating net segment lengths (the flat model of Davis [5] and the hierarchical one of Stroobandt [14] of which the last one is easily combinable with our multi-terminal net model). Although the new estimates for source-sink pairs are quite close to the old wire length estimates, we observed that the scaling behaviour (as a function of circuit size) fundamentally differs when the influence of the multi-terminal nets increases ($\gamma \ll 1/2$). For the first time, we are also able to model Steiner tree lengths as a combination of the right net segment lengths. Naturally, the longest wires in the Steiner tree estimations fundamentally differ from those for the previous net segment estimates.

Overall, our new Steiner length estimate seems to be quite accurate (in comparison to experimental Steiner length measurements) which validates (i) the net segment length estimation based on Stroobandt’s results [14, 8], (ii) the multi-terminal net model, and (iii) the model for combining net segments to Steiner trees.

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