The Capability Hardware-Enhanced RISC Instructions (CHERI) CPU architecture is motivated by the need for security and performance properties that are needed in the modern software ecosystem. CHERI achieves a reduced instruction set computer (RISC) approach to capabilities, providing much of the computer and operating system security while maintaining hardware compatibility. CHERI's protection, efficient simulation implementation of advanced security models, enhancing defenses, and design principles are realized in Capability Hardware-Enhanced RISC Instructions (CHERI) and the temporally enhanced security language and system (TESLA) abstract syntax. CHERI adopts a carefully crafted, while modern, approach to securing embedded systems and advanced operating systems. CHERI is designed for the future, so core architectural features are critical.

CHERI achieves reduced instruction set computer (RISC) approach to capabilities, providing much of the computer and operating system security while maintaining hardware compatibility. CHERI's protection, efficient simulation implementation of advanced security models, enhancing defenses, and design principles are realized in Capability Hardware-Enhanced RISC Instructions (CHERI) and the temporally enhanced security language and system (TESLA) abstract syntax. CHERI adopts a carefully crafted, while modern, approach to securing embedded systems and advanced operating systems. CHERI is designed for the future, so core architectural features are critical.

CHERI adds a reduced instruction set computer (RISC) approach to capabilities, providing much of the computer and operating system security while maintaining hardware compatibility. CHERI's protection, efficient simulation implementation of advanced security models, enhancing defenses, and design principles are realized in Capability Hardware-Enhanced RISC Instructions (CHERI) and the temporally enhanced security language and system (TESLA) abstract syntax. CHERI adopts a carefully crafted, while modern, approach to securing embedded systems and advanced operating systems. CHERI is designed for the future, so core architectural features are critical.

CHERI adds a reduced instruction set computer (RISC) approach to capabilities, providing much of the computer and operating system security while maintaining hardware compatibility. CHERI's protection, efficient simulation implementation of advanced security models, enhancing defenses, and design principles are realized in Capability Hardware-Enhanced RISC Instructions (CHERI) and the temporally enhanced security language and system (TESLA) abstract syntax. CHERI adopts a carefully crafted, while modern, approach to securing embedded systems and advanced operating systems. CHERI is designed for the future, so core architectural features are critical.

CHERI adds a reduced instruction set computer (RISC) approach to capabilities, providing much of the computer and operating system security while maintaining hardware compatibility. CHERI's protection, efficient simulation implementation of advanced security models, enhancing defenses, and design principles are realized in Capability Hardware-Enhanced RISC Instructions (CHERI) and the temporally enhanced security language and system (TESLA) abstract syntax. CHERI adopts a carefully crafted, while modern, approach to securing embedded systems and advanced operating systems. CHERI is designed for the future, so core architectural features are critical.