# Implications of Electronics Technology Trends to Algorithm Design

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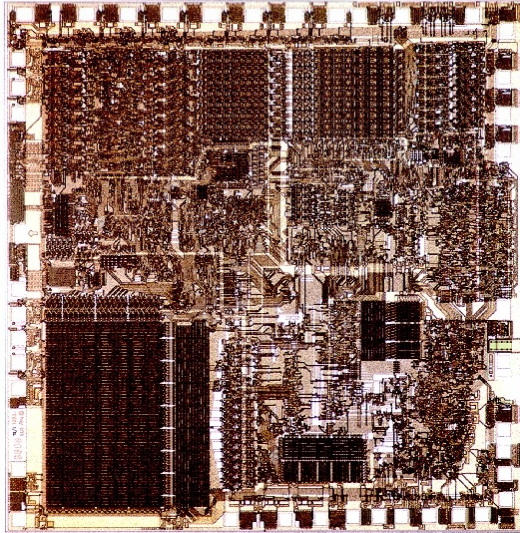Computer Architecture Group

# Overview

Pivotal changes in hardware

Algorithm mapping in space and time

Predicting complexity of communication

Conclusions & Research Questions

# Wires stopped scaling 40 years ago



Intel 8086 (1978)
29,000 transistors
3μm process



Intel Pentium-4 (2000)
42,000,000 transistors
0.18μm process

# Computation vs. Communication

- Relative power consumed

| technology node | 130nm CMOS (2006) | 45nm CMOS (2008) |
|---|---|---|
| transfer 32b across-chip | 20 computations | 57 computations |
| transfer 32b off-chip | 260 computations | 1300 computations |

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# Virtualization of Interconnect
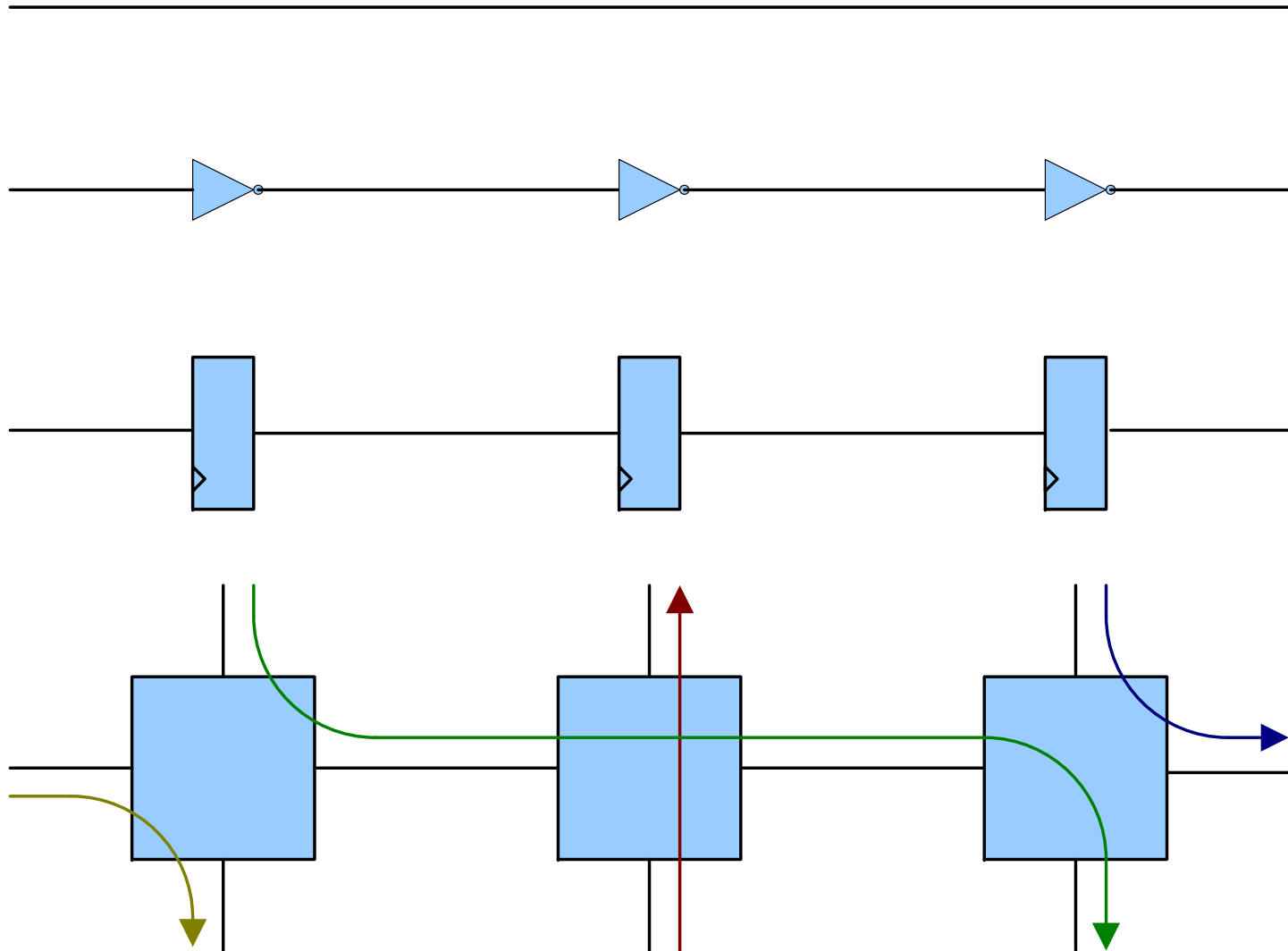
# Observation

*technology scaling favours transistors over wires*
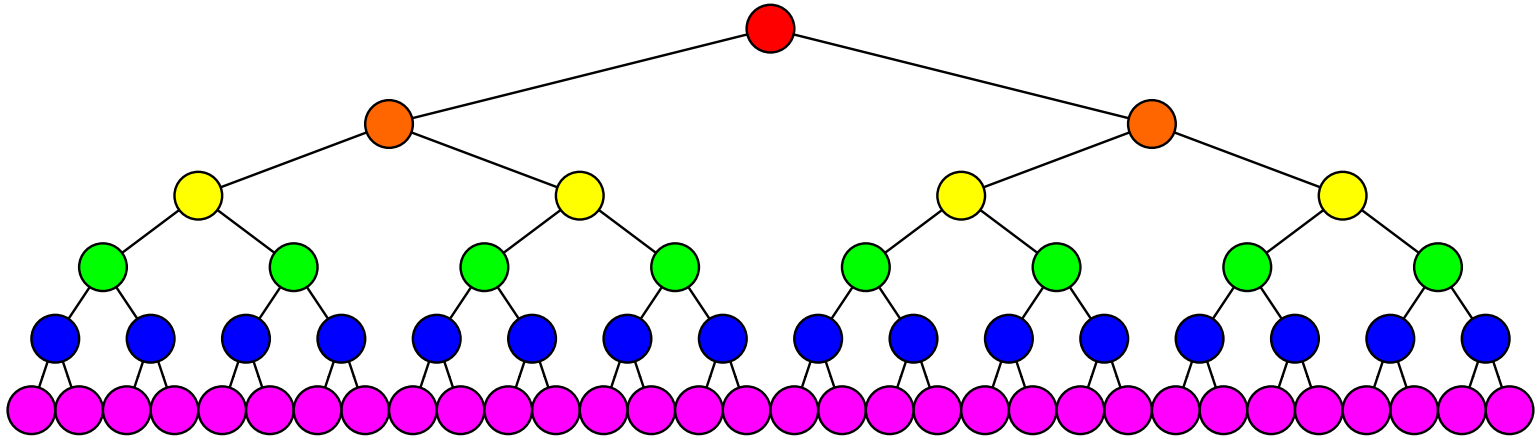
# Overview

Pivotal changes in hardware

**Algorithm mapping in space and time**

Predicting complexity of communication

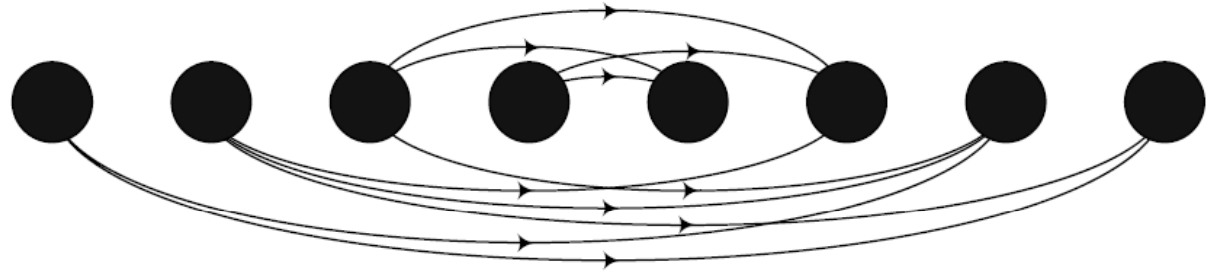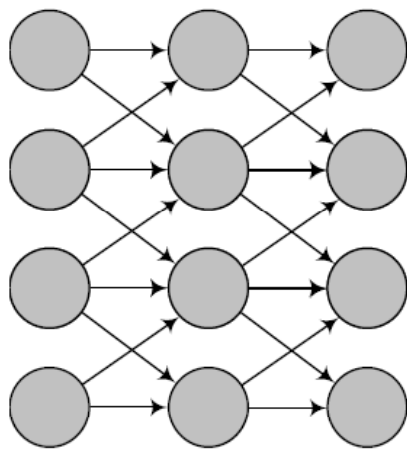Conclusions & Research Questions

# Embedding a Binary Tree into 2D
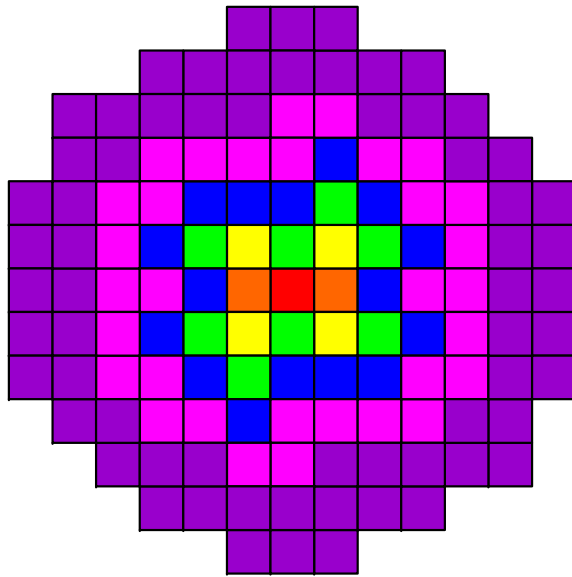
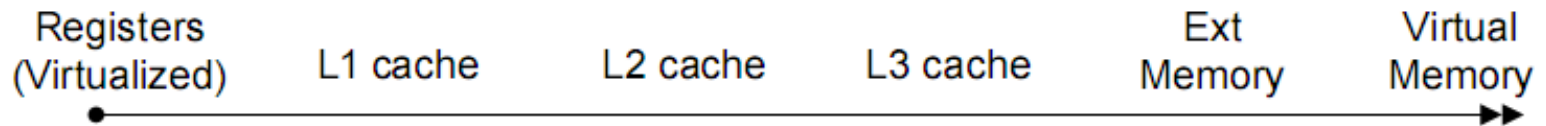**Binary Tree Traversal**

No Communication Cost: $O(\log n)$

Random Placement: $O(\sqrt{n}.\log n)$

Optimal Placement: $O(\sqrt{n})$

# Spatio-Temporal Interconnect



Time

Registers (Virtualized) — L1 cache — L2 cache — L3 cache — Ext Memory — Virtual Memory

Temporal Distance and Cost

# Overview
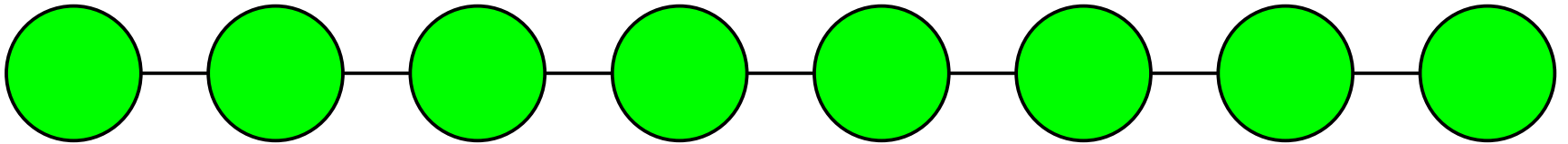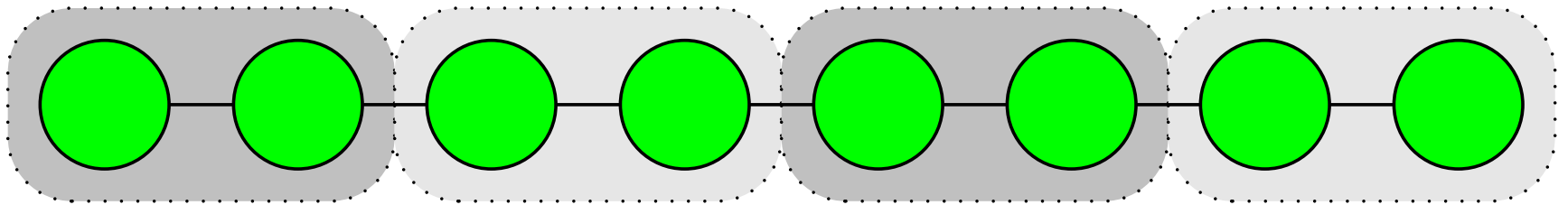
# Software Graphs

- Dynamic data dependency graph
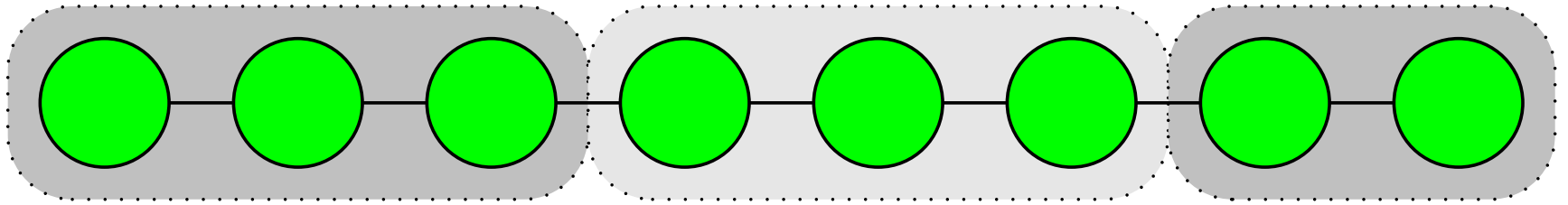  - graph representation of computation data dependencies
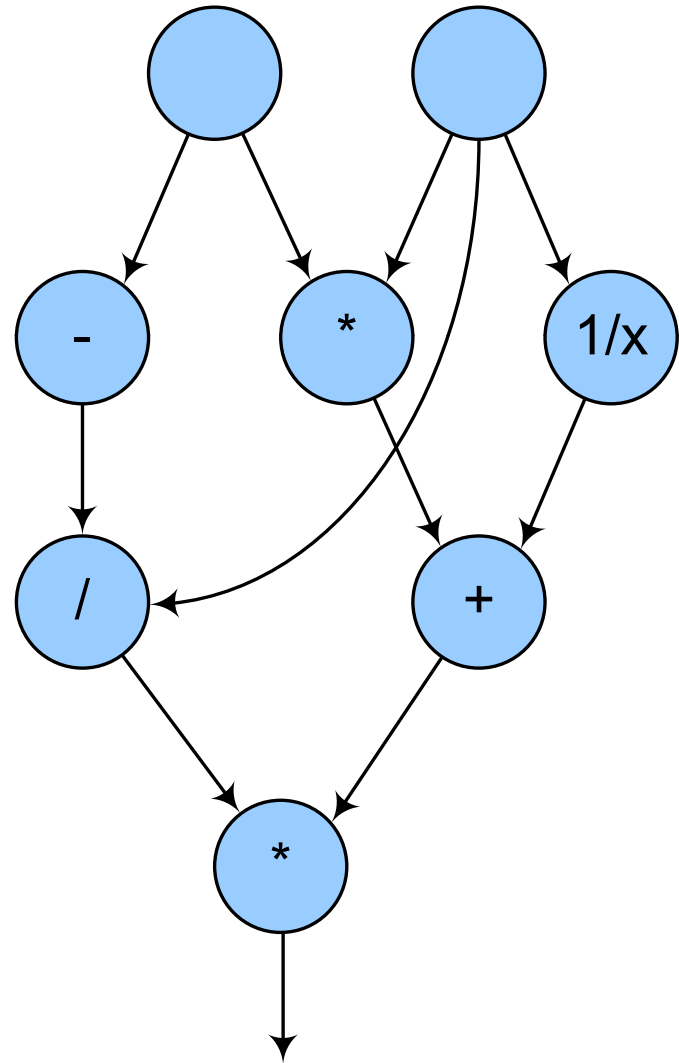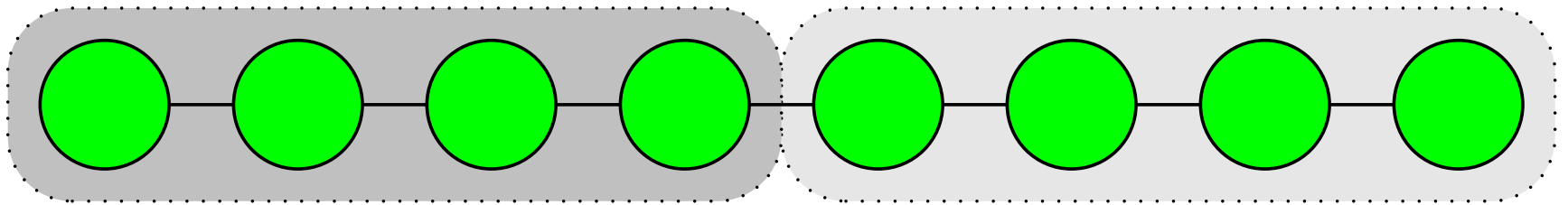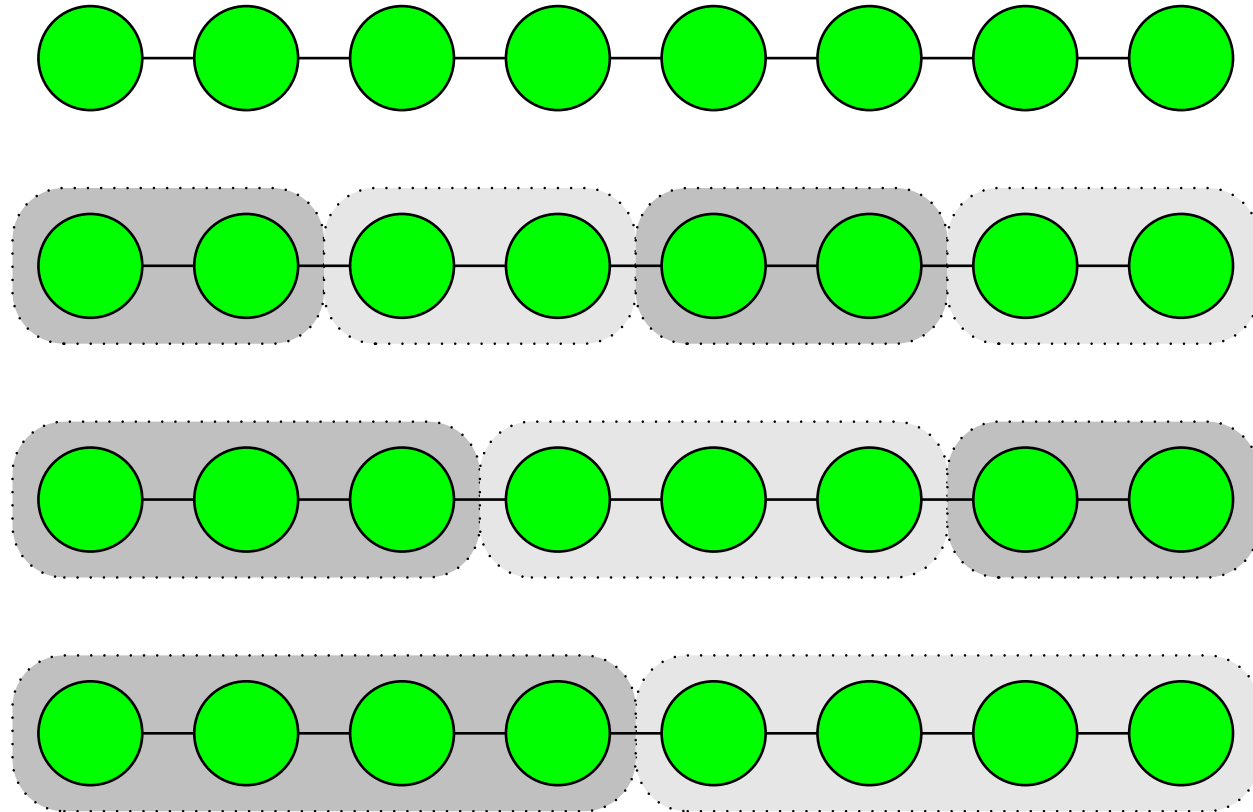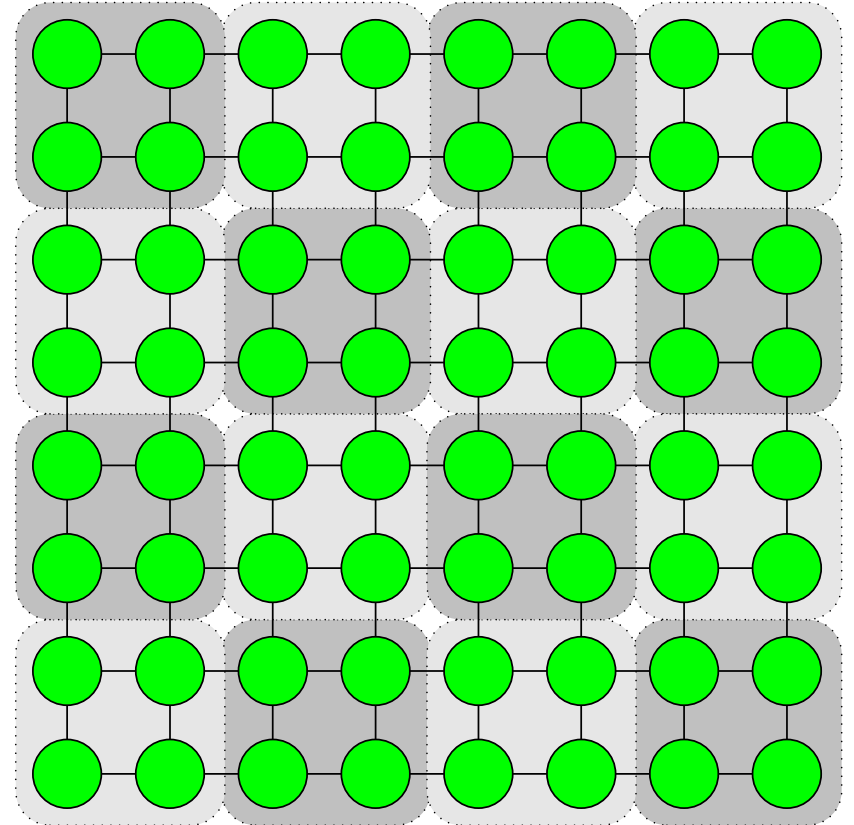
# Box Counting

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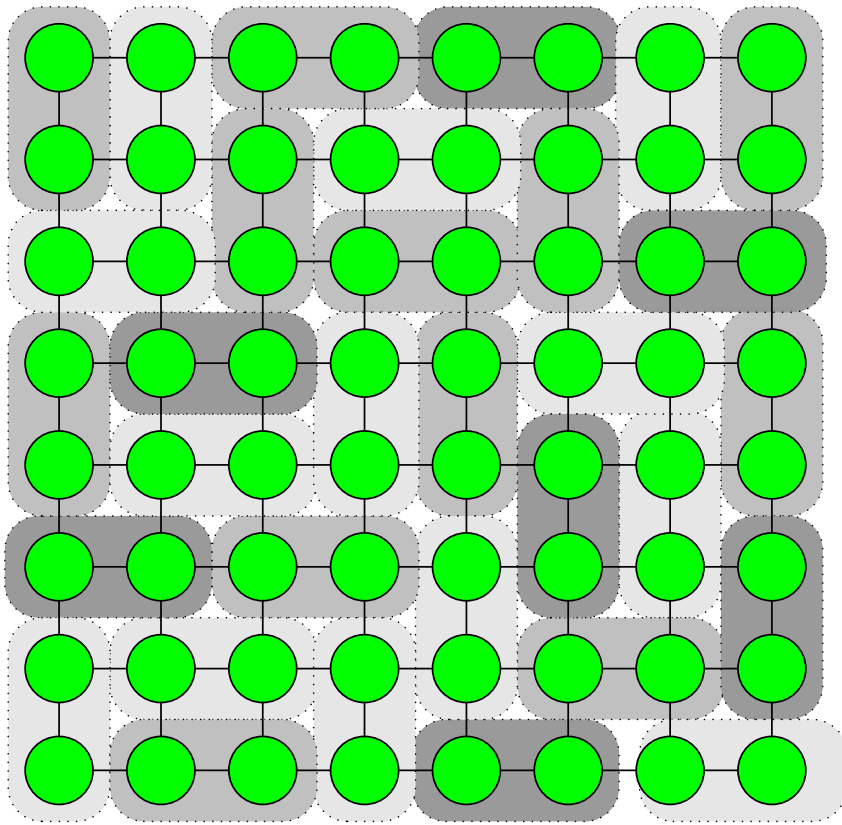
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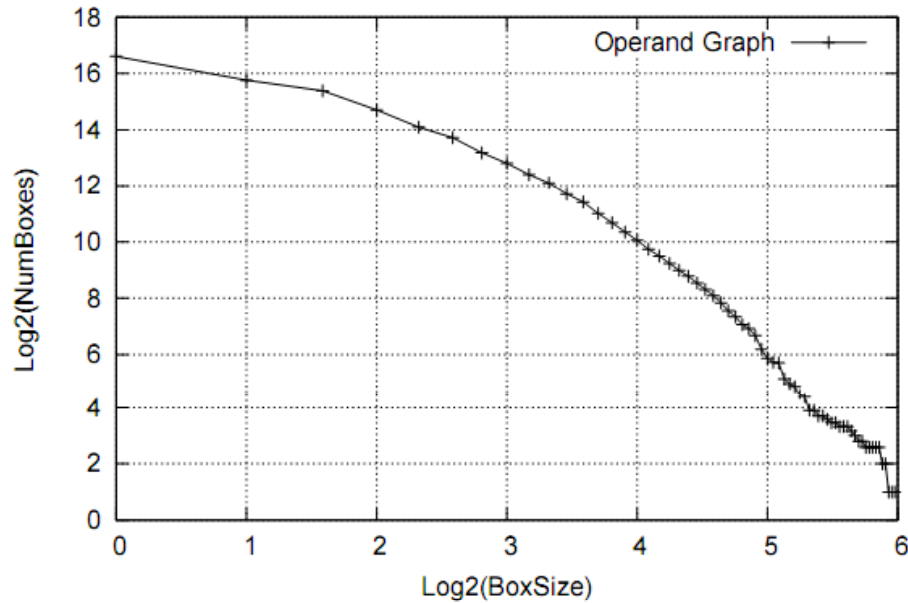


$$N \propto 1/L$$

# Box Counting



$$N \propto 1/L^2$$

# Fractal Communication in SW



Box Counting Measure: qsort — Operand Graph

Box Counting Measure: gsmdec — Dynamic Data Dependency Graph, Linear fit, slope=-2.4267
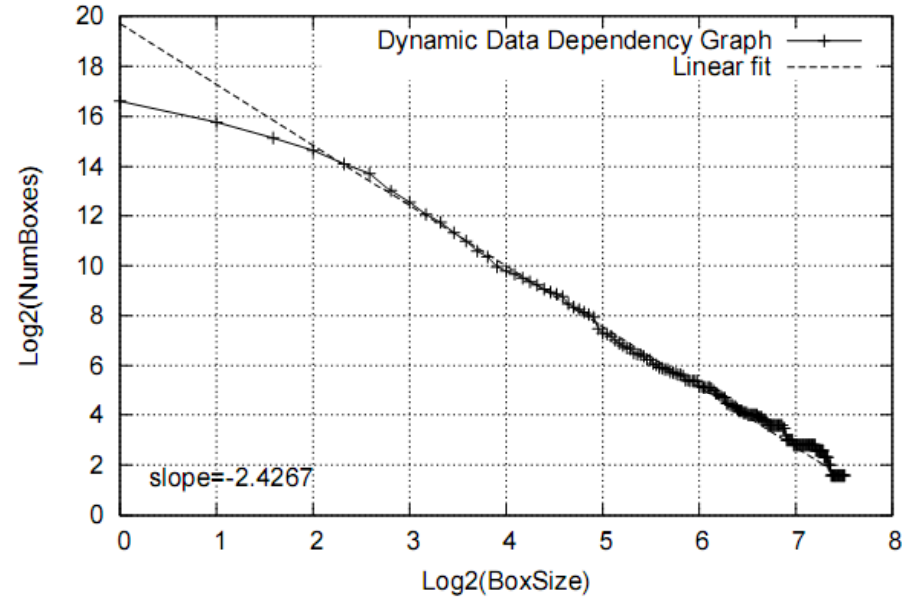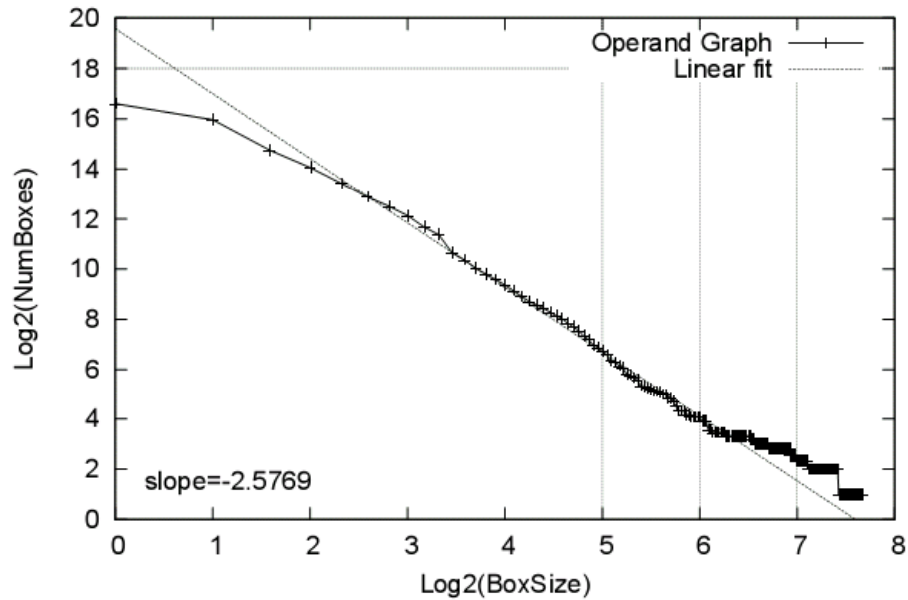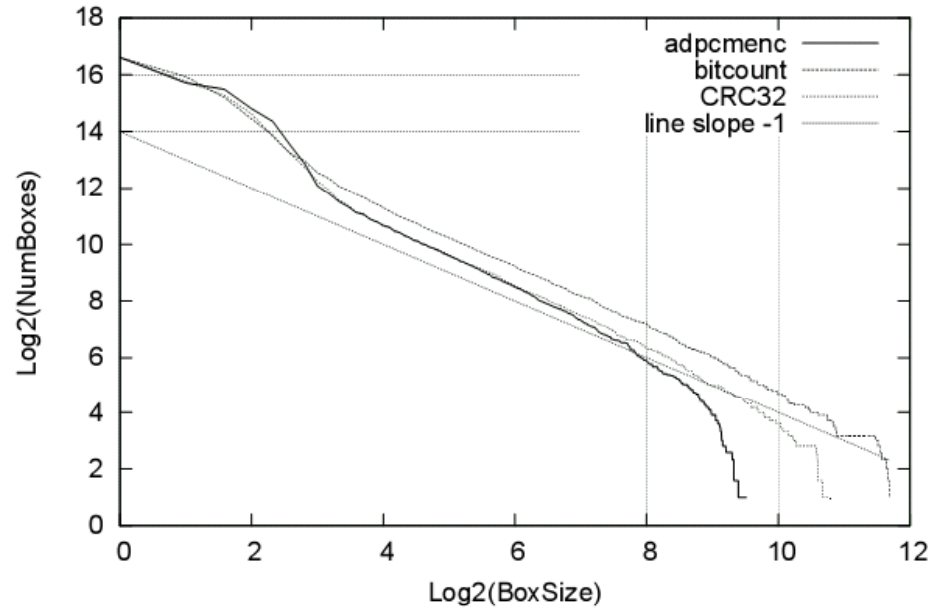
# Fractal Communication in SW



Box Counting Measure: lame

Box Counting Measure: adpcmenc, bitcount, CRC32

# A Scalability Metric

*Locality of communication in an algorithm is related to its fractal dimensionality*

# Temporal Interconnect



Temporal Distance Distribution: ls
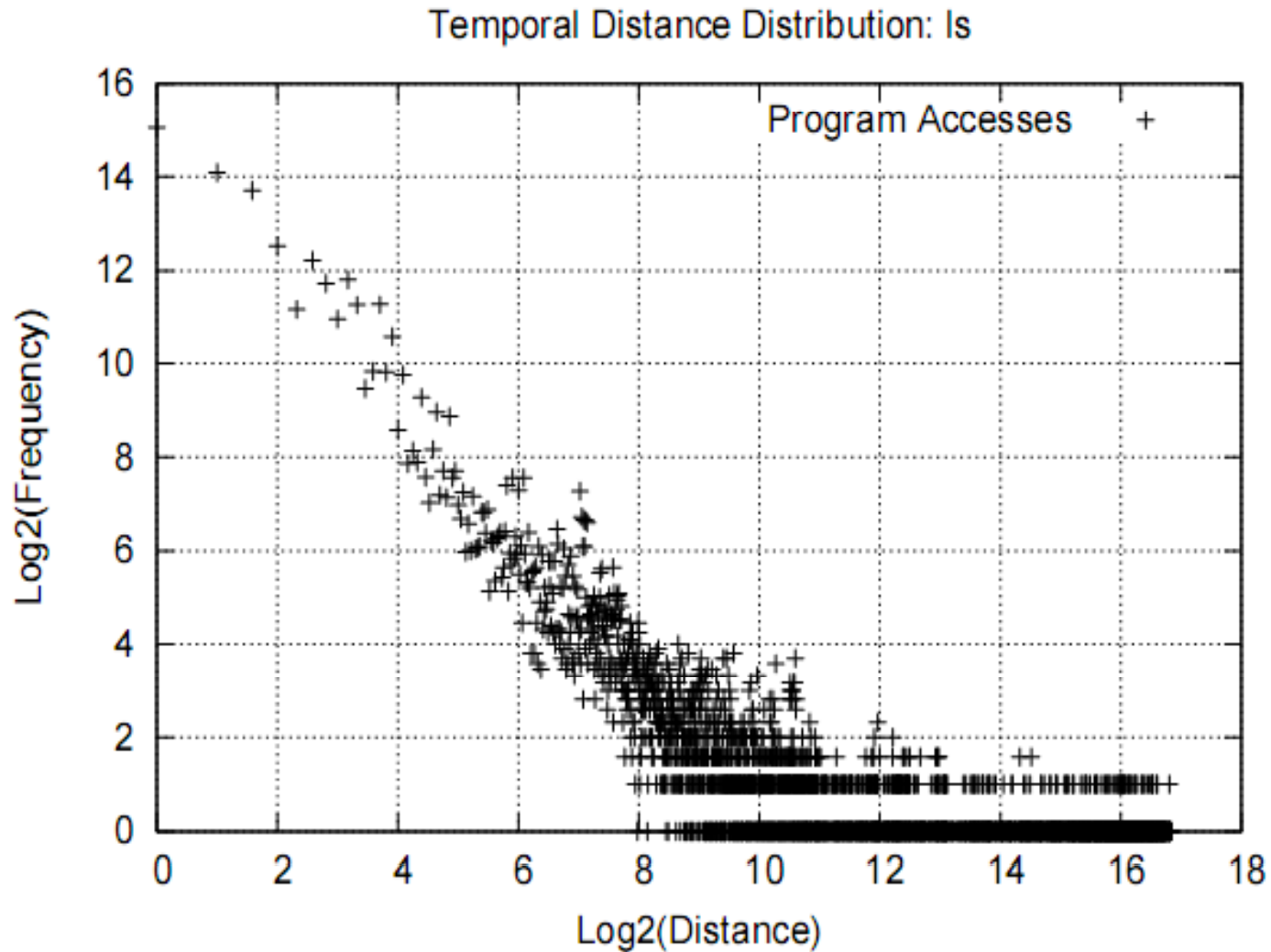
# Level-2 unified cache utilisation
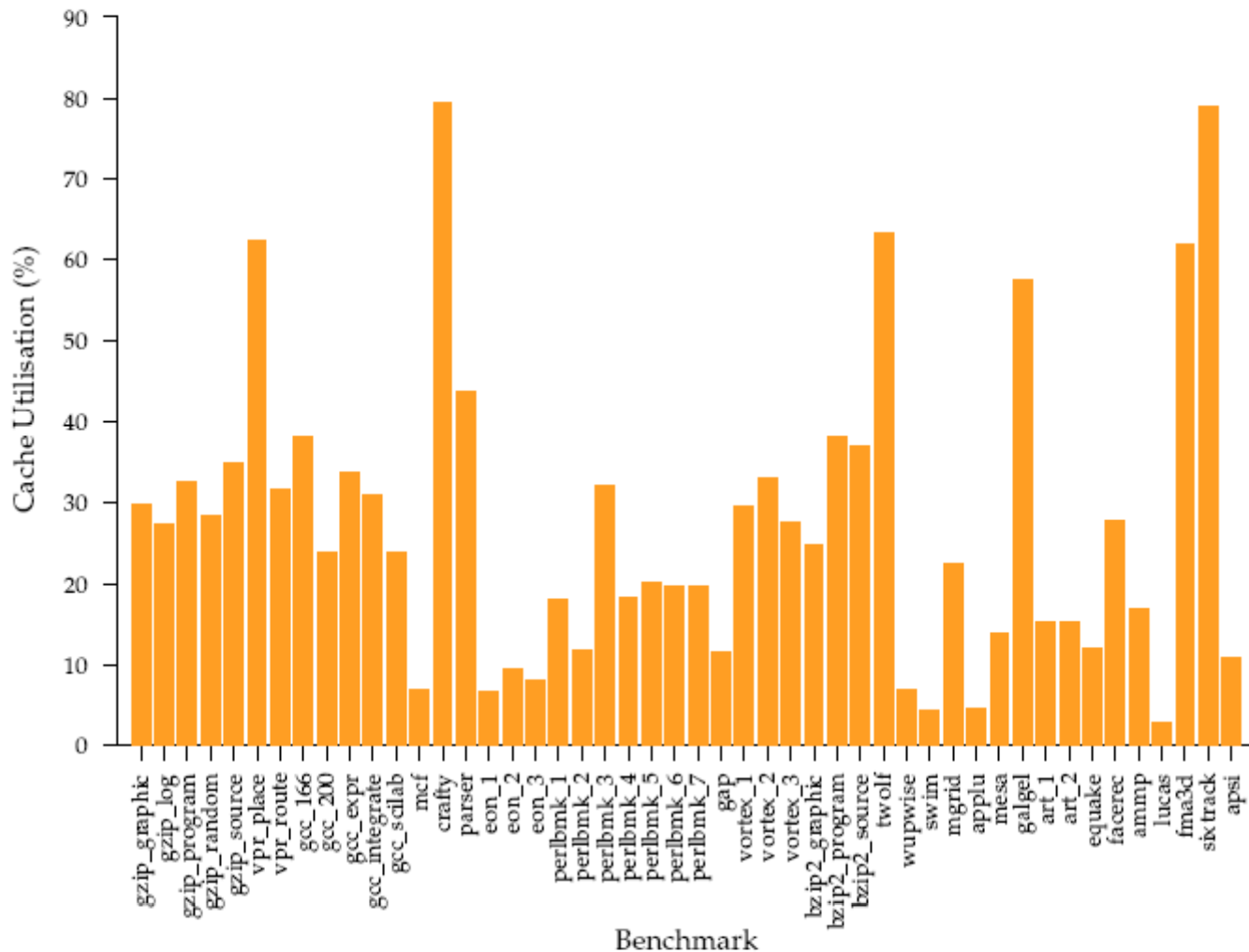


From James Srinivasan, University of Cambridge, Computer Laboratory

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**Conclusions & Research Questions**

# Conclusions and Research Questions

- Software exhibits fractal locality
  - Can we exploit this behaviour?
  - Can we automatically reduce communication complexity/dimensionality?
  - How tight are the dimensionality constraints on communication statistics?

# Conclusions and Research Questions

- Memory as temporal interconnect
  - Similarities to spatial interconnect / switch
  - Can we leverage our statistical models to design better temporal interconnect?
- Unification of views
  - Data is routed in space and time
  - What new techniques can we develop by unifying spatial and temporal communication?

# Conclusions and Research Questions

- Technology scaling favours transistors over wires
  - Position of data and computation within the chip will be critical
  - Will have a fundamental impact on the way we design efficient algorithms
  - Need to do more computation to optimise communication
  - Fractal dimensionality of communication will be an important metric in assessing new algorithms