Timing Diagrams — Old and New

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16th February 1993

1 The Port Controller

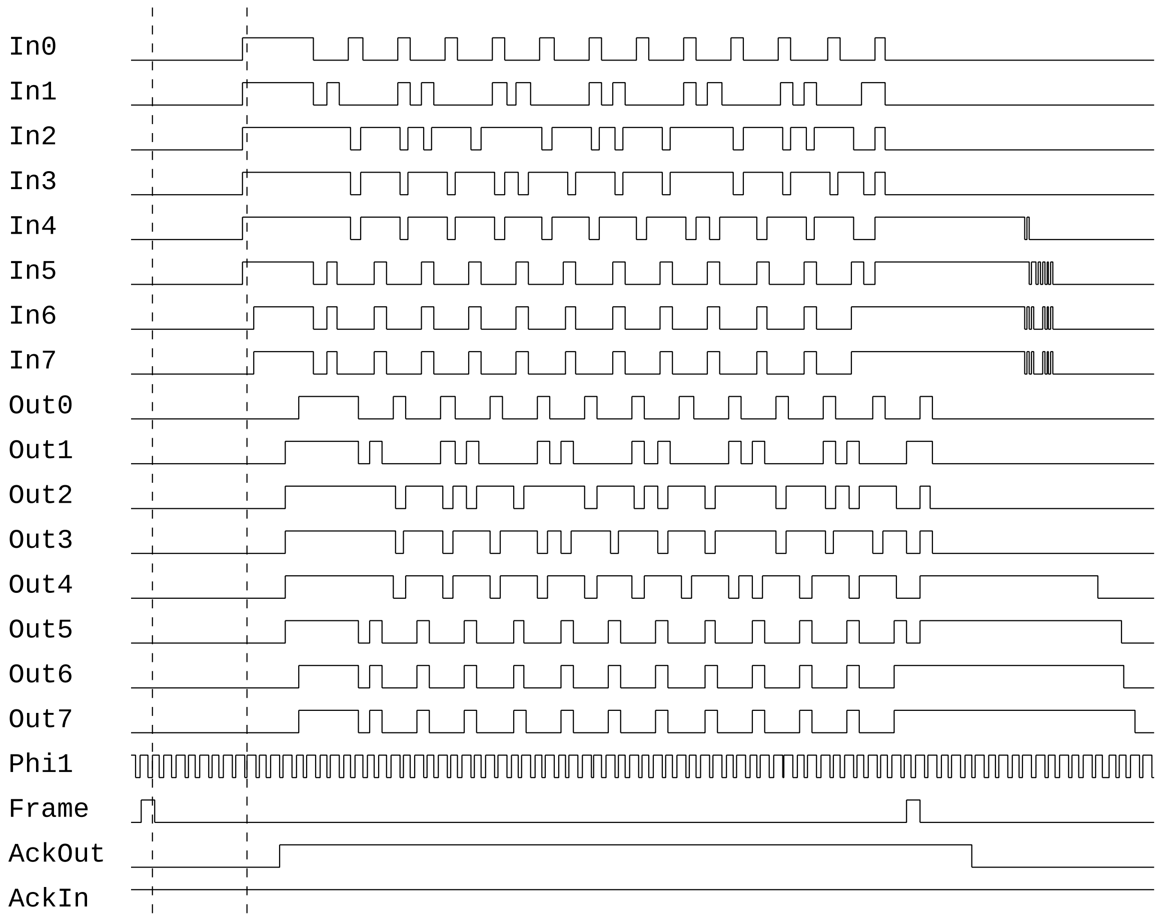

Figure 1: Timing Diagram

Figure 1 shows the timing diagram for a cell entering and leaving a port controller (Phi1 is the clock). 'Frame' pulses are generated as the result of every 64^{th} rising clock edge, and any device wishing to send a cell into the fabric must generate the first byte of the cell (the routeing byte) as a result of the eight rising clock edge after the one which created the 'frame' pulse, so that the fabric can latch that byte on the next rising edge. i.e. it must be generated as result of the seventh rising clock edge after the frame pulse is latched by the device. The dotted lines on figures 1 and 2 and the lines marked A and B on figure 3 show the rising clock edges which are used to latch the 'frame' signal and the first byte of the cell. They are 8 clock cycles appart.

The ACK signal in this case is propagated from AckIn to AckOut as soon as the fabric decides that the cell has been routed successfully.

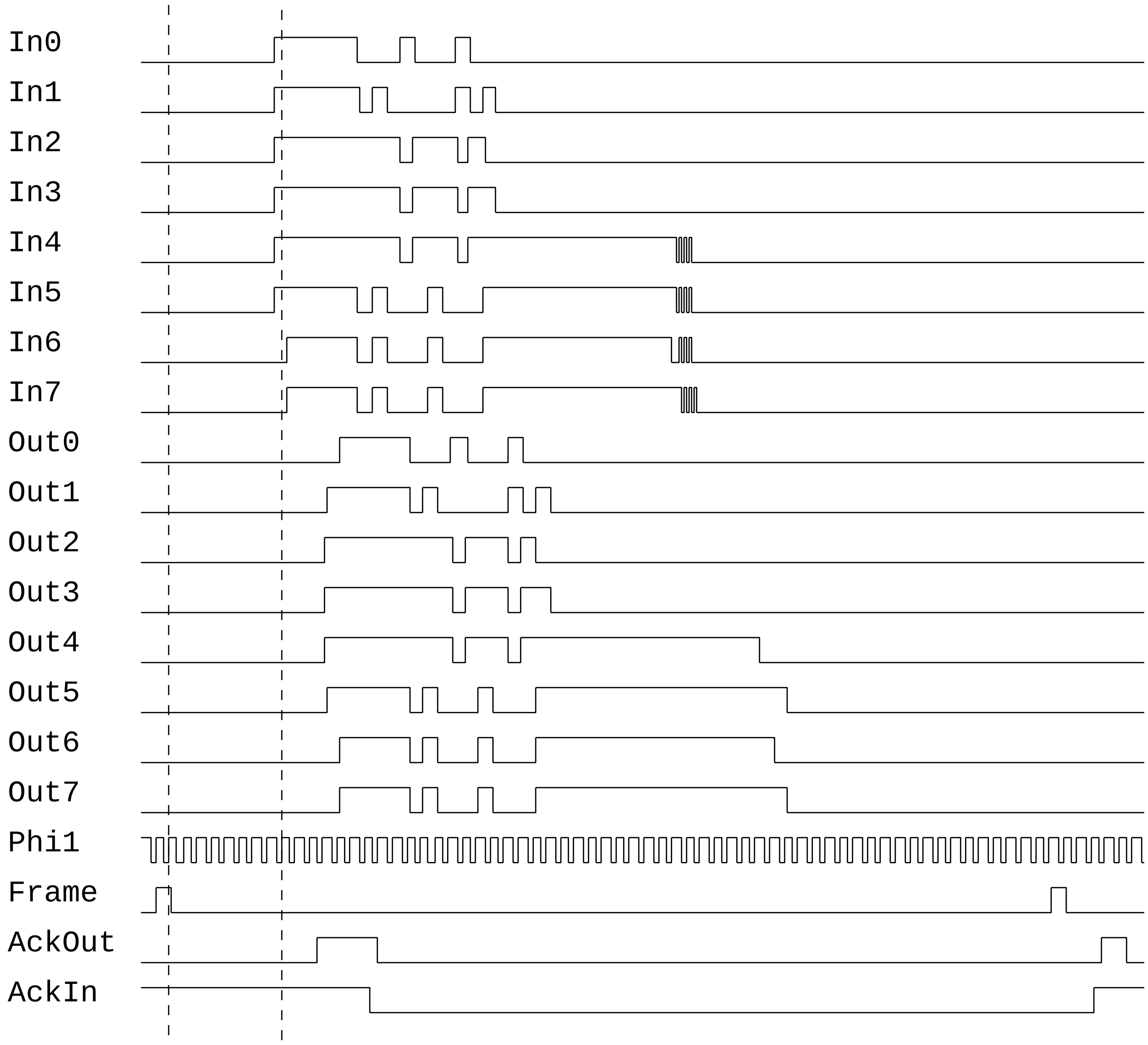

Figure 2: Timing Diagram (for a NACKed Cell)

Figure 2 shows the timing diagram for a cell, which has been NACKed, entering and leaving a port controller. As before, the AckIn signal is propagated through the fabric as it finishes the arbitration process. In this case, however, the receiving circuit decides that it cannot accept the cell (as a result of its FIFO being full) and therefore pulls AckIn low. This is propagated to AckOut and the sending circuit aborts the cell after about 15 bytes.

2 The New Acknowledgement Protocol

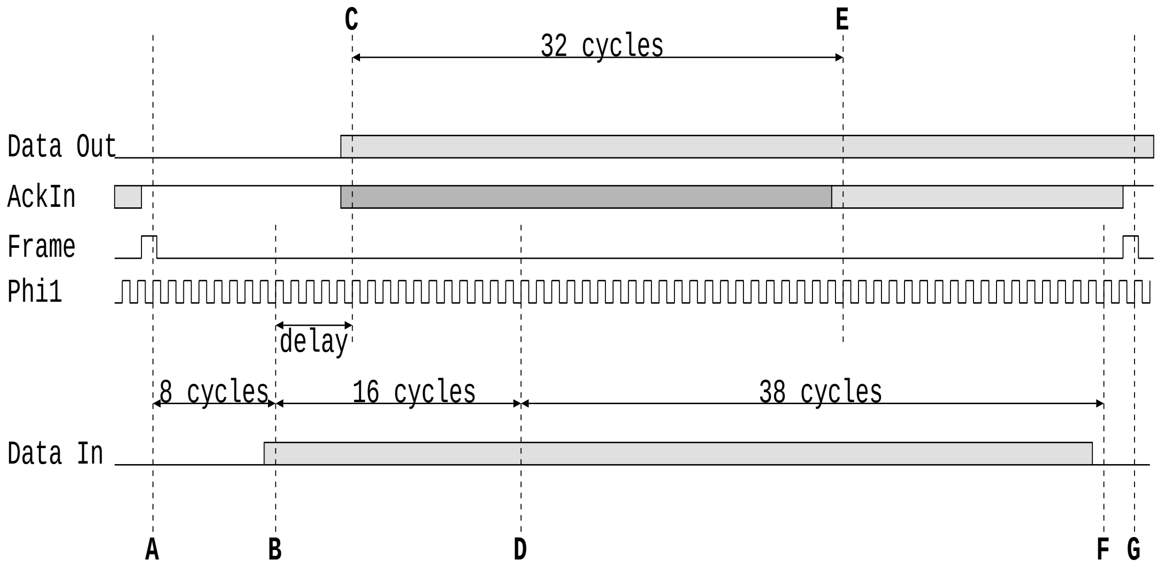

Figure 3: Timing Diagram (for the new protocol)

Figure 3 shows the timing diagram from the new acknowledgement protocol. As before, a cell must be presented to the fabric 8 clock cycles after the 'frame start' pulse (as shown between lines A and B in figure 3). The receiving device will see the cell some number of clock cycles later (B to C on the figure) — the number being dependent on the depth of the fabric (see document 25: Delay Through the Switch Fabric). The receiver then has 32 clock cycles to decide whether or not it is going to acknowledge the cell (C to E) after which it must retain the state of AckIn until the next 'frame start' pulse (E to G) when it must set AckIn high (indicating acknowledgement — as in the period A to C).

The transmitting device should wait 16 clock cycles after it presents the cell to the fabric (B to D) and the look at the AckOut signal coming out of the fabric. If at any point after this and before the end of the cell is put into the fabric (D to F), this signal goes low then the cell has been NACKed otherwise is has been ACKed.

It *is* valid to hold the AckIn line low after the 'frame start' pulse provide it isn't pulled high before the next 'frame start' signal. This indicates that any cell presented to the receiving device will be NACKed.

It is also valid to hold the AckIn line high between 'frame start' pulses, indicating that any cell presented will be ACKed.

3 Notes

The timing diagrams showing in figures 1 and 2 were downloaded from a logic analyser connected to a fairisle port controller. These therefore show the protocol used by the existing port controllers and not other devices. Figure 3 shows a proposed protocol which has not been implemented yet, but it is intended that all devices which will connect to a switch fabric in the future will use this new protocol.