Verilog Syntax Chart - Sheet 1 of 2
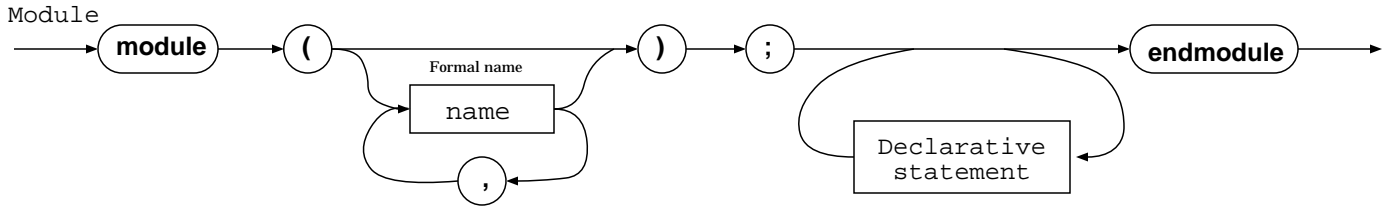
These two sheets give the syntax
of the learners' subset of Verilog.

A Verilog file consists of a set of modules.

Module

module → (→ [Formal name: name] , →) → ; → [Declarative statement] → endmodule

Declarative Statement

input
output
inout
wire
reg

Net and port declarations

Range

Name , → ;

initial
always

Behavioural specifications

Behavioural Statement

Continuous assignment

assign → name → = → Expression → ;

Component/module instantiation.

Component name: name → Instance name: name → (→ Positional argument passing: Expression , →) → ;

(→ . → Formal name: name → (→ Expression →) →)
Associative argument passing
,

Range

[→ num → : → num →]
[→ num →]