Parallel Hardware Merge Sorter

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Hardware Sorter

• Sorting algorithm is important
  – One of the most used algorithms
  – Database, search engine, MapReduce, et al.
  – Highly data dependent

• Hardware sorting accelerator
  – Unknown random data distribution
  – cache < data set < memory
  – No good solution until very recent
Type of Sorters

Parallel (Sorting Network)

- 13
- 10
- 11
- 9
- 25
- 20
- 21
- 10

- 9
- 10
- 10
- 11
- 13
- 20
- 21
- 25

- Block operation
- High sorting rate
- Limited data set

Sequential Sorter

- 9, 10, 11, 13
- 10, 20, 21, 25

- Stream operation
- Low sorting rate (1 number/cycle)
- Unlimited data set

Can we combine them?
Naïve Parallel Merger

Does NOT work because data may distribute unevenly!
Naïve Parallel Merger

For it to work properly:
- A **1-cycle** feedback sorting network.
- A FIFO with **variable** data rate.
Fast Feedback using Bitonic Merger

2 Num/cycle
0 5 7 11
4 6 10 23

1 3 9 21
2 8 15 25
2 Num/cycle

Bitonic Partial Merger

4 Num/cycle

0~4 Num/cycle
6 7
7 10
10 11
11 23
2 9

0~4 Num/cycle
3 15
8 21
9 25

Single cycle feedback delay, fully pipelined, minimal area overhead.
Area Efficient Multirate FIFO

Not a standard FIFO or shifter design.
Area Efficient Multirate FIFO

Diagram showing the operation of the Area Efficient Multirate FIFO, with two rate converters, one for 2 number/cycle and the other for 0~4 number/cycle.

- Cycle 1: Selecting 3 numbers
  - 13, 14 → 17, 18, 19 → 17, 18, 19, 20

- Cycle 2: Selecting 2 numbers
  - 11, 12 → 13, 14 → 14, 15, 16, 17

- Cycle 3: Selecting 4 numbers
  - 9, 10 → 11, 15, 12 → 12, 13, 14, 15

- Cycle 4: Selecting 0 numbers
  - 7, 8 → 9, 10, 11 → 9, 10, 11

The diagram includes the numbers processed in each cycle, showing the flow of data through the FIFO.
Multirate Merger (Implementation)
Parallel Merge-Tree

Accumulated input rate equates with the maximal output rate, both are 8 num/cycle.
Rate Mismatch

Two ways to handle rate mismatch:

- Increase input rate to the maximal output rate in each merger (previous work).
  - (J. Casper and K. Olukotun. “Hardware acceleration of database operations.” FPGA 2014)

- Allow stall and use long FIFOs to reduce stall rate. (this paper)
Rate Mismatch

Significant increase of accumulated input rate! For a 4 num/cycle merge tree, the accumulated input rate is **16 num/cycle!**
Reducing Stalls using FIFO

Stall rate vs. FIFO depth

FPGA area overhead

A single SRL is a 16-bit shifter.
There is no extra cost to increase depth to 16.
Sorting Skewed Data

Skewed data: data with uneven distribution, causing duplicated data.
Sorting Skewed Data

Statically configure comparators to choose the even distribution. When possible, use duplicated data to balance FIFOs.
Sorting Skewed Data

Poisson distribution

Zipfian distribution
Scalability Analysis

Parallel Merge-Tree in a Virtex-7 XC7VX485T FPGA

<table>
<thead>
<tr>
<th>Ports</th>
<th>Period (ns)</th>
<th>Frequency (MHz)</th>
<th>Register</th>
<th>LUT</th>
<th>SRL</th>
<th>Stall Rate</th>
<th>Data Rate (Number/cycle)</th>
<th>Data Rate (Gb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>4.02</td>
<td>248.5</td>
<td>328 (0.05%)</td>
<td>853 (0.28%)</td>
<td>132</td>
<td>1.75%</td>
<td>1.97</td>
<td>31.3</td>
</tr>
<tr>
<td>4</td>
<td>4.69</td>
<td>213.1</td>
<td>1534 (0.25%)</td>
<td>4278 (1.41%)</td>
<td>528</td>
<td>2.16%</td>
<td>3.91</td>
<td>53.4</td>
</tr>
<tr>
<td>8</td>
<td>6.12</td>
<td>163.3</td>
<td>5287 (0.87%)</td>
<td>16016 (5.28%)</td>
<td>1608</td>
<td>2.56%</td>
<td>7.80</td>
<td>81.5</td>
</tr>
<tr>
<td>16</td>
<td>7.50</td>
<td>133.4</td>
<td>16299 (2.68%)</td>
<td>47001 (15.48%)</td>
<td>4238</td>
<td>2.74%</td>
<td>15.56</td>
<td>132.9</td>
</tr>
<tr>
<td>32</td>
<td>10.08</td>
<td>99.2</td>
<td>45445 (7.48%)</td>
<td>142179 (46.83%)</td>
<td>11379</td>
<td>2.98%</td>
<td>31.05</td>
<td>197.1</td>
</tr>
</tbody>
</table>

Utilization of FPGA Resource

Minimal Clock Period (ns)
Sorting Time Estimation

\[ t_{\text{PMT}(P)} \sim (1 - \bar{r}_{\text{stall}}) \cdot \frac{N}{P} \log_P N \]

\[ = \frac{(1 - \bar{r}_{\text{stall}})}{P \log P} \cdot N \log N \]

160x Speed up (PMT32)
# Related Sorters (Rough Estimation)

<table>
<thead>
<tr>
<th>Sorter</th>
<th>Type</th>
<th>Device</th>
<th>Clk Freq</th>
<th>Rate</th>
<th>Time est (1G N)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel Merge Module</td>
<td>Parallel merger</td>
<td>ASIC</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>No stall, single stage full comparator.</td>
</tr>
<tr>
<td>(1989) [1]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High BW Sort Merge Unit</td>
<td>Parallel merger</td>
<td>Xilinx Virtex-6</td>
<td>200M</td>
<td>6 num/cycle 4 seq/pass ?</td>
<td>2.5G cycle 12.5 sec</td>
<td>No stall. Need 5-port memory support, 6.14x memory BW.</td>
</tr>
<tr>
<td>(2014) [2]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel Merge-Tree</td>
<td>Parallel merger</td>
<td>Xilinx Virtex-7</td>
<td>99M</td>
<td>32 num/cycle 32 seq/pass</td>
<td>0.19G cycle 1.88 sec</td>
<td>Allow stall, 1x memory BW.</td>
</tr>
<tr>
<td>(2016) [This]</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>FPGASort</td>
<td>Sequential merger</td>
<td>Xilinx Virtex-5</td>
<td>252M</td>
<td>1 num/cycle 2 seq/pass</td>
<td>30G cycle 2 min</td>
<td></td>
</tr>
<tr>
<td>(2011) [3]</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Tree-merger</td>
<td>Sequential merger</td>
<td>Xilinx Virtex-5</td>
<td>273M</td>
<td>1 num/cycle 102 seq/pass</td>
<td>4.5G cycle 16.5 sec</td>
<td></td>
</tr>
<tr>
<td>(2011) [3]</td>
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</tbody>
</table>

Conclusion and Future Works

• A scalable parallel merge-tree
  – Merge multiple sorted sequences
  – High sorting speed-up
    • High sorting rate
    • Merging multiple sequences in each pass
  – Scalable area and speed performance
    • Allowing stall
  – Strong tolerance to skewed data

• Future work
  – Full sorting system with connection to host computer
  – Data scheduling and compression over PCIe