From Channel Slicing to Spatial Division Multiplex for Asynchronous Networks-on-Chip

Wei Song
Supervisor: Doug Edwards
Advisor: Christopher Harrison
Background: Networks-on-Chip

- CPU
- FPU
- Memory
- Bridge
- Timer
- Ethernet
- USB
- I/O
- Network Interface
- Processor
- Router
Synchronous/Asynchronous

- Synchronous
  - Clock triggered
  - Fast
  - Small
  - Power Consuming
  - Sensitive to variation
  - Complex clock tree

- Asynchronous
  - Handshake
  - Slow !!
  - Large
  - Power Efficient
  - Tolerance to variation
  - No clock tree
Why asynchronous is slow?

Advantages: data on all sub-channels are synchronized, ease the time division multiple access (TDMA) techniques, such as virtual channel and TDMA

Drawbacks: low speed (66% on CD)
ChSlice: implementation

2-bit

C

C

2-bit

C

C

16

d_i

ack_i

2-bit

d_o

ack_o

2-bit

d_i0

d_o0

ack_i0

ack_o0

2-bit

d_i15

d_o15

ack_i15

ack_o15
Flow control

![Flow control diagram]

- **Head:** Starts at the top and moves downward.
- **Routing:** Moves from left to right, indicating the sequence of data transmission.
- **Data:** Represents the actual data being transmitted, following the head and routing patterns.
- **Sub-channels:** Show the division of data into smaller segments for transmission.

The diagram illustrates how data is controlled and directed through channels over time, ensuring efficient and orderly transmission in the context of advanced processor technology.
Router: structure

5 input ports
5 output ports
ctl

arbiter

ack_i_0
ack_i_0
d_i_0
ack_o_0
d_o_0

d_i_4
16
80
ack_i_4
ack_o_4
d_o_4

cntl
arbiter
arbiter

5 output ports
Speed and Area

![Graphs showing the relationship between data width and router area or cycle period for Channel Sliced and Synchronized cases.](image-url)
Future Work

• Implementation of a Spatial Division Multiplex (SDM) router (under test)
  – Switch structure
    • Clos Switch Networks
  – Path scheduling algorithm
    • random round-robin -> random arbitration

• Quality of Services support
  – Two switch structure in one router
Publications


Question?
## Compare with other routers

<table>
<thead>
<tr>
<th></th>
<th>Tech (nm)</th>
<th>Period (ns)</th>
<th>Period (Hz)</th>
<th>Pipeline Style</th>
<th>Other</th>
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<tbody>
<tr>
<td>Sliced Wormhole</td>
<td>130</td>
<td>2.2</td>
<td>450M</td>
<td>4-phase 1-of-4</td>
<td>Standard cell</td>
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<tr>
<td>Synchronized Wormhole</td>
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<td>2.8</td>
<td>360M</td>
<td>4-phase 1-of-4</td>
<td>Standard cell</td>
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<td>ANoC</td>
<td>130</td>
<td>4.0</td>
<td>250M</td>
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<td>Customized Cell Lib</td>
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<td>ASPIN</td>
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<td>0.88</td>
<td>1.13G</td>
<td>Dual-Rail / Bundled-Data</td>
<td>Customized Cell Lib</td>
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<td>QNoC</td>
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<td>Delay line</td>
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<td>408M</td>
<td>Synchronous circuit</td>
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</tbody>
</table>
Crossbar, Benes, Clos

Area

VCs per port

crossbar
benes
clos_snb
clos_rnb