Untethering the Rocket-Chip

Producing a stand-alone lowRISC SoC

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Background

• Rocket-chip
  – An open-source SoC from UC Berkeley
  – Rocket core
    • RISC-V 64 ISA
    • 5/6 stage single-issue in-order processor
    • Non-blocking L1 D$
    • Performance comparable to ARM Cortex-A5
    • Chisel (RTL, OO, functional)
    • Zynq FPGA (ARM A9), Linux bootable
    • Full cross-compilation tool chain
Rocket-Chip

Issues:
1. Must work with a companion core (ARM).
2. No direct IO (peripheral) support.
3. No direct bootloading.
Memory Mapped IO (1)
Memory Mapped IO (2)

Diagram showing the flow of data and meta signals through different stages (1 to 4) involving mem.req, mem.grant, io.req, and io.grant, with additional signals like meta, data, replay, and ioaddr.
Bootloading Procedure (1)

Memory: 0x00000000 – 0x3FFFFFFF
IO space: 0x40000000 – 0xFFFFFFFF
DDR3 memory in IO space (bypass L1/L2)

Copy Linux image from SD to DDR3 using IO space (bypassing L1/L2).
Bootloading Procedure (2)

Memory: 0x40000000 – 0x7FFFFFFF -> 0x00000000 – 0x3FFFFFFF
IO space: 0x80000000 – 0xFFFFFFFF
DDR3 memory in memory space

Remap DDR3 to Memory 0x00000000 – 0x3FFFFFFF
Reset L1/L2 (clean any instructions from bootloader)
All must be coded in one cache line (16 insns)
Bootloading Procedure (3)

Memory: 0x40000000 – 0x7FFFFFFF ->
0x00000000 – 0x3FFFFFFF
IO space: 0x80000000 – 0xFFFFFFFF
DDR3 memory in memory space

0x00000000 – 0x3FFFFFFF
0x80000000 – 0xFFFFFFFF

AXI Bus

L2 Cache Bus

L2 & Coherence Manager

L2 & Coherence Manager

L2 & Coherence Manager

Arbiter

DMA

DMA

UART

SD

Chisel

SystemVerilog

On-FPGA

Boot Ram

Memory Controller

TileLink/AXI-Lite

0x80000000

TileLink/AXI

0x00000000

0x40000000

Boot Image

Linux image

Uncached TileLink for MMIO