GAELS Project Meeting
Automatic Data Path Extraction

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15/11/2013

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Content

• Tool Flow
• Progress
  – Updated Type Calculation
  – Detailed FSM classification
  – Automatic Data Path Extraction
  – Preliminary Partition Analysis
• Future Works
• Conclusion
A large RTL system can be partitioned into multi sub-design connected by data channels with variable data-rates.
Flow inside Async Synthesizer

- Verilog Parser
- Elaborator
- SDFG Generation
- FSM Extraction
- Data Path Extraction
- GALS Partition
- Async Netlist
- Constraint Generation
- Cell Libs
Progress from Last Meeting

• Automatic FSM classification
  – Add more types in SDFG
  – Automatic identify FSMs, counters and flags.

• Automatic data path extraction
  – Removing control arcs
  – Trim the SDFG afterwards

• Preliminary partition analysis
  – All data outputs have variable data rate
always @(posedge clk or negedge rstn)
if(~rstn)
  state <= R;
else
  state <= state_nxt;
always @(state or cnt) // next state
if(cnt == 0)
  case(state)
    R: state_nxt = YR;
    YR: state_nxt = G;
    G: state_nxt = YG;
    default: state_nxt = R;
  endcase // case (state)
else
  state_nxt = state;
always @(posedge clk or negedge rstn)
if(~rstn)
  cnt <= 0;
else if(cnt == 0)
  case(state)
    R: cnt <= 2;
    YR: cnt <= 49;
    G: cnt <= 4;
    default: cnt <= 49;
  endcase // case (state)
else
  cnt <= cnt - 1;
assign red = state == R ? 1 : 0;
assign green = state == G ? 1 : 0;
assign yellow =
  (state == YR || state == YG) ? 1 : 0;
Add Extra Arc Types

• Old typing systems
  – Data
  – Control
  – Clock; Reset

• New typing system
  – Self-loop; Calculation; Assign; Data*
  – Compare; Equate; Logic; Address; Control*
  – Clock; Reset
Recognition Criteria

- State machine
  - Self (equate); Out(equate); In(!data)

- Counter
  - Self(Calculate); Out(equate | compare | logic); In(!data)

- Address
  - Self(default); Out(address); In(!data)

- Flag
  - Self(All); Out(logic); In(!data)

- Other
  - Self(All); Out(control); in(!data)
SUMMARY:
In this extraction, 2074 nodes has been scanned, in which 120 nodes are registers.

In total 30 FSM controllers has been found in 101 potential FSM registers.

The extracted FSMs are listed below:

[1] dwb_biu/aborted_r FLAG
[2] dwb_biu/valid_div CNT|FLAG
[3] iwb_biu/aborted_r FLAG
[4] iwb_biu/previous_complete FLAG
[5] iwb_biu/valid_div CNT|FLAG
[6] or1200_cpu/or1200_ctrl/sig_syscall FLAG
[7] or1200_cpu/or1200_ctrl/sig_trap FLAG
[8] or1200_cpu/or1200_except/delayed_.iee FLAG
[9] or1200_cpu/or1200_except/ex_dslot FLAG
[10] or1200_cpu/or1200_except/except_type FSM|ADR

[11] or1200_cpu/or1200_except/extend.Flush FSM|FLAG

[12] or1200_cpu/or1200_except/state FSM|FLAG
[13] or1200_cpu/or1200_if/saved FLAG
[14] or1200_cpu/or1200_mult_mac/div_free FLAG
[15] or1200_cpu/or1200_operandmuxes/saved_a FLAG
[16] or1200_cpu/or1200_operandmuxes/saved_b FLAG
[17] or1200_dc_top/or1200_dc_fsm/cache_inhibit FLAG
Data Path Extraction

RTL

Parser

Abstract Syntax Tree

Signal-Level DFG

Remove Control Arcs

Graph Trimming

Data Paths

Data path extraction
module GCD (Clock, Reset, Load, A, B, Done, Y);
input Clock, Reset, Load;
input [7:0] A, B;
output Done;
output [7:0] Y;
reg A_lessthan_B, Done;
reg [7:0] A_New, A_Hold, B_Hold, Y;

always @(posedge Clock)
    if(Reset) begin
        A_Hold = 0;
        B_Hold = 0;
    end
end

always @(posedge Clock)
    if(Load) begin
        A_Hold = A;
        B_Hold = B;
    end
end

always @(posedge Clock)
    if(A_Hold || B_Hold) begin
        A_lessthan_B = A_Hold <= B_Hold;
        A_New = A_Hold - B_Hold;
    end
end

always @(posedge Clock)
    if(Reset || Load) begin
        A_Hold = A_Hold;
    end
end

always @(posedge Clock)
    if(Reset || Load) begin
        A_lessthan_B = A_lessthan_B;
        A_New = A_New;
    end
end

endmodule
Remove Control Arcs
Trim the SDFG
Permutation Module (SHA-3)
Large Scale Designs
## Performance

<table>
<thead>
<tr>
<th>Design</th>
<th>Signal-level DFG</th>
<th>Extracted data path</th>
<th>Running time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I/O</td>
<td>Module</td>
<td>Signal</td>
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<tr>
<td>OR1200</td>
<td>52</td>
<td>37</td>
<td>2074</td>
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<td>RSD</td>
<td>7</td>
<td>24</td>
<td>1063</td>
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<td>NOVA</td>
<td>19</td>
<td>140</td>
<td>7043</td>
</tr>
</tbody>
</table>
Partition Detection

Classify each output port as fixed rate (through wire or pipeline) or variable rate (variable data, FSM control, FSM).

A module with most output ports with variable rate is considered a potential partition.
Partition Detection Report

pixel_generator (module vga_pgen) with rate $0.470588 < 0.8$:
- hsync_o: 0 [pixel_generator/hsync_o:data-pipeline]
- cc0_adr_o: 0 [through wire]
- cc1_adr_o: 0 [through wire]
- stat_acmp: 1 [pixel_generator/stat_acmp:self-fsm:ctl-
  fsm(pixel_generator/stat_acmp)]
- blank_o: 0 [pixel_generator/blank_o:data-pipeline]

wbm/clut_sw_fifo (module vga_fifo_aw4_dw1) with rate $1 >= 0.8$:
- aempty: 1 [wbm_ack_i_P:data-pipeline]
  [pixel_generator/color_proc/vdat_buffer_rreq:ctl-
  fsm(pixel_generator/rgb_fifo/nword]
- full: 1 [wbm/clut_sw_fifo/full:ctl-
  fsm(wbm/stb_o,wbm/clut_sw_fifo/rp,wbm/clut_sw_fifo/wp)]
- empty: 1 [wbm/clut_sw_fifo/empty:ctl-
  fsm(wbm/stb_o,wbm/clut_sw_fifo/rp,wbm/clut_sw_fifo/wp)]
- nword: 1 [wbm/clut_sw_fifo/nword:ctl-fsm(wbm/stb_o)]
- afull: 1 [wbm_ack_i_P:data-pipeline]
  [pixel_generator/color_proc/vdat_buffer_rreq:ctl-
  fsm(pixel_generator/rgb_fifo/nword,pixel_generator/color_proc/colcnt]
Future Works

- Partition Detection
  - Rather than evaluate all output ports, evaluate only data output ports.
  - Replace the pattern detection with data rate estimation (possibly need state space analyses)
  - Back-annotate data rate to data path graph
  - Interface recognition (mem, FIFO, handshake, bus, etc)
Conclusion

Utilizing signal-level data flow graph, the sync Verilog synthesizer is able to:

– Detect and classify controllers
– Detect data paths
– Detect potential partitions (preliminary)