Maths and asynchronous pipelines: some facts, figures, and structure

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A systematic way of studying design spaces applied to timed and untimed, bundled, 2– and 4phase asynchronous latch controllers.

This work relies heavily on well documented real circuits published by the asynchronous community.

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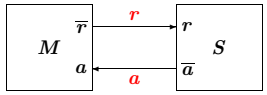
Our grateful thanks to both.

Webster and System Description

A system is a collection of objects ... coordinated according to logical or scientific principles.

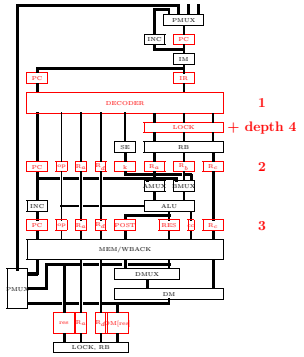
Rules of the CCS game:

1. Agree protocol e.g. $\overline{req}/ack$
2. Agree distinct line names: *line*
3. Map signals to their lines



$$M = \overline{r}\,.\quad a\,.\,M$$
$$\Downarrow \qquad \Uparrow \qquad \text{H'SHAKES}$$
$$S = r\,.\,t\!\!\not{d}\,.\,\overline{a}\,.\,S$$
$$SYS_0 = (\ M \mid S\ ) \setminus PRIVATE$$
$$PRIVATE = \{\ r,\ a\ \}$$

Modelling Manchester Amulets

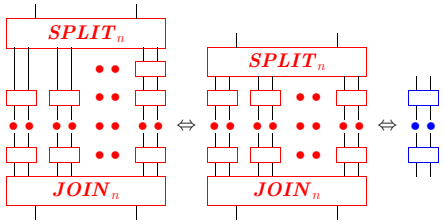


CONTROL SIGNALS ONLY

Datapipeline minimises to same FSM *whatever* its width... NB Arithmetic units, muxes etc just delay and contribute no variety.

Equivalent mental model

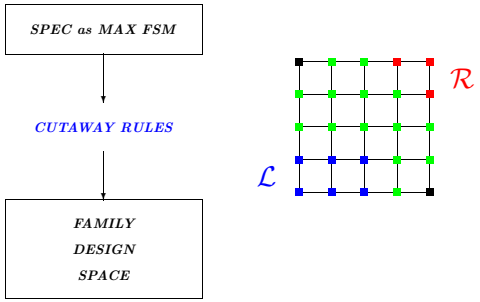
We may replace the structured parallel pipeline by a single pipeline of the same depth.



A real help when modelling both *it* and the *rest* of the processor.

NB it probably won't (99%) behave *quite* like the pipeline stage you designed: but we can predict the new behaviour.

Essence of the approach

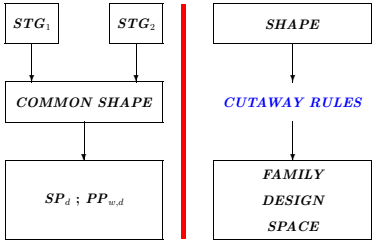


- Generate *max* FSM
  - ... generate $\mathcal{L}$ cuts and $\mathcal{R}$ cuts
  - ... DESIGN SPACE = $\mathcal{L}$ o $\mathcal{R}$
  - ... $\mathcal{L}$ o $\mathcal{R}$ relate family behaviours

What has been done

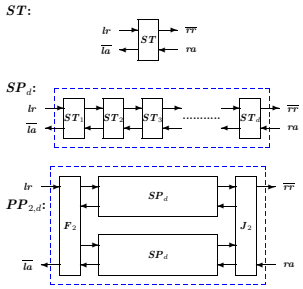
1. 50 published designs ⇒ common shape (FSM) notation so designs can be compared and related.
2. MAX shape; $\mathcal{L}/\mathcal{R}$ cutaways yield FAMILIES of shapes. The cuts order and relate these shapes.
3. STRUCTURE: $\mathcal{L}$ and $\mathcal{R}$ cuts are persistent. They predict pipeline behaviours, occupancy, ..., even relate to circuit properties.
4. DESIGN SPACE: $\mathcal{L}$ o $\mathcal{R}$ tableau shows the whole design space One 10 $\times$ 25 segment has been implemented by standard tools from the CCS shapes. Some new designs look good.

STGs/Abstract Shape/Family



1. Several STGs → same shape
2. We can define the maximal shape
   ... and its derivative family
3. from cuts we can
   ... relate and order shapes
   ... even predict properties

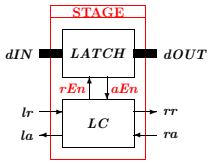
Pipeline experiments w,d=1..8



Common outputs $\overline{rr}/\overline{la}$ and Inputs lr/ra

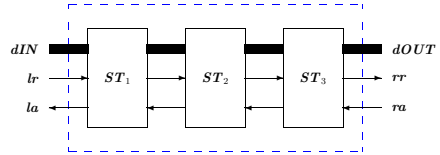
1. A common set of signals means we can compare and relate designs
2. We clearly require a compositional notation

A look inside



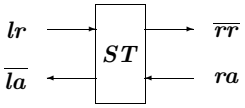
The latch is responsible for holding the captured value from bus ***dIN*** and the latch controller is responsible for its safety.

NB Bus[1]



[1] It is usual to omit the bus from the specification since the stage operates independently the data value.

2phase pipeline stages



$L = lr\ .\ \overline{la}\ .\ L \qquad R = \overline{rr}\ .\ ra\ .\ R$

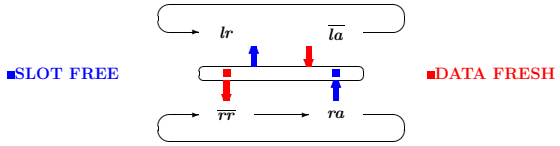
Reading . as *and some time later*:

lr • $\overline{la}$
• ⇒ arbitrary internal delay
ra • $\overline{rr}$

$\overline{la}$ • lr
• ⇒ arbitrary external delay
$\overline{rr}$ • ra

1. CCS is an apt notation and
2. figures out all interleavings

Max 2phase stage MP



CONSTRAINTS:

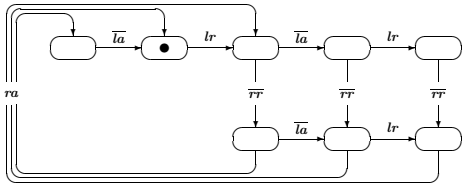
Don't overwrite unread data:
pD ≺ lr ≺ ?get slot ≺ capt

Don't pass on stale data:
?fresh data ≺ $\overline{rr}$ ≺ ra ≺ pass

$$
\begin{aligned}
L &= lr\ .\ get_{\blacksquare}\ .\ \text{capt}\ .\ put_{\blacksquare}\ .\ \overline{la}\ .\ L \\
R &= get_{\blacksquare}\ .\ \overline{rr}\ .\ ra\ .\ \text{pass}\ .\ put_{\blacksquare}\ .\ R \\
MP &= (\ L \mid {\scriptstyle\blacksquare} \mid {\scriptstyle\blacksquare} \mid R\ ) \\
&\quad \setminus \{\ get_{\blacksquare},\ put_{\blacksquare},\ get_{\blacksquare},\ put_{\blacksquare}\ \}
\end{aligned}
$$

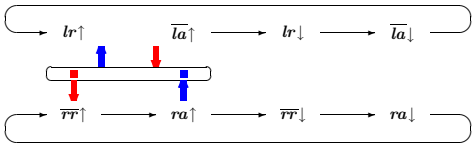
Minimised *MP* and its *SHAPE*

Minimised FSM for *MP*— trace free



SHAPE: a clutterfree version

Max 4phase stage



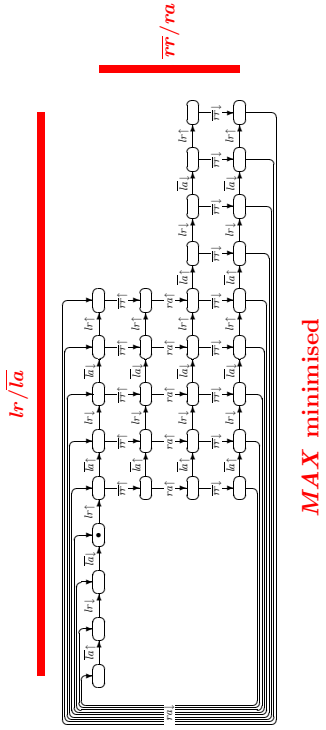
$L = lr\uparrow \ . \ get_{\blacksquare} \ . \ capt \ . \ put_{\blacksquare} \ . \ \overline{la}\uparrow \ . \ lr\downarrow \ . \ \overline{la}\downarrow \ . \ L$

$R = get_{\blacksquare} \ . \ \overline{rr}\uparrow \ . \ ra\uparrow \ . \ pass \ . \ put_{\blacksquare} \ . \ \overline{rr}\downarrow \ . \ \overline{ra}\downarrow \ . \ R$

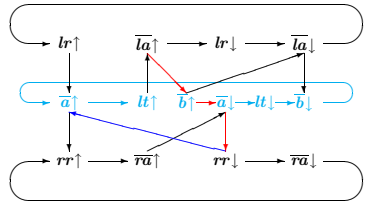
$LC_{max} = (\ L \mid \blacksquare \mid \blacksquare \mid R\ ) \setminus \{\ get_{\blacksquare}, put_{\blacksquare}, get_{\blacksquare}, put_{\blacksquare}\ \}$

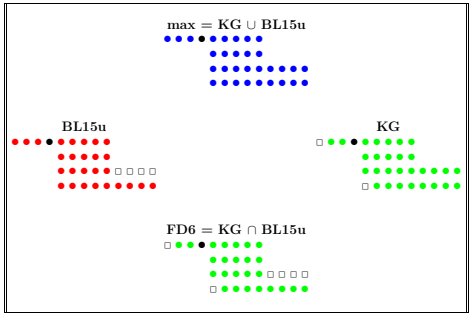
4phase protocol obeys:

1. ALWAYS POSSIBLE ONLY $lr\uparrow$
2. $lr\uparrow \prec \overline{la}\uparrow \prec lr\downarrow \prec \overline{la}\downarrow$ L
3. $\overline{rr}\uparrow \prec ra\uparrow \prec \overline{rr}\downarrow \prec \overline{ra}\downarrow$ .... R
4. ■ $pass_{k-1} \prec capt_k$ $\quad k > 1$
   ■ $capt_k \prec pass_k$



STG: Furber and Day, sect 6

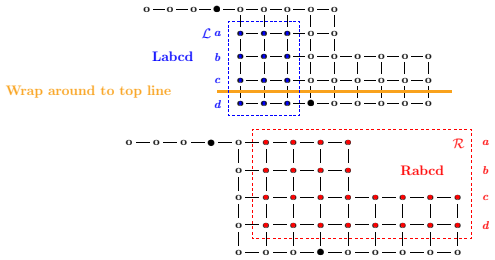




STG vs Shape abstraction

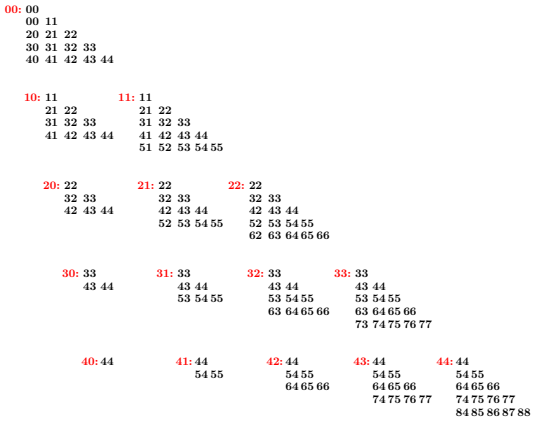
Design	Hiding	Depth d					
		1	2	3	4	5	6
MP	yes	8	12	16	20	24	28
FD4	*lt*	16	44	116	304	796	2084
	yes	12	20	28	36	44	52
FD5	*lt,a*	28	112	448	1792	7168	28672
	yes	18	32	48	64	80	96
FD6	*lt,a,b*	62	450	3290	*24053	*175858	*1285718
	yes	26	44	60	76	92	108
FD7	*lt,a,b*	42	260	1604	9886	*60930	*375536
	yes	22	40	56	72	88	104
MAX	yes	32	48	64	80	96	112

Cutaways from *MAX*



1. $\mathcal{L}$ has 35 members; $\mathcal{R}$ has 140: a design space of 4900 shapes
2. When $\mathcal{L}$ and $\mathcal{R}$ overlap/abut, the 4phase protocol no longer holds (deadlock)
3. We generate related families via structured subsets.

Lattice of $\mathcal{R}$cuts ABcut × CDcuts



Symmetric (complementary).
Pleasingly coherent and complete.

Families of designs

Can we tie up $\mathcal{L}/\mathcal{R}$ choices with various design styles?

UNTIMED DI/SI (250)

1. inputs must be accepted
2. outputs may be delayed

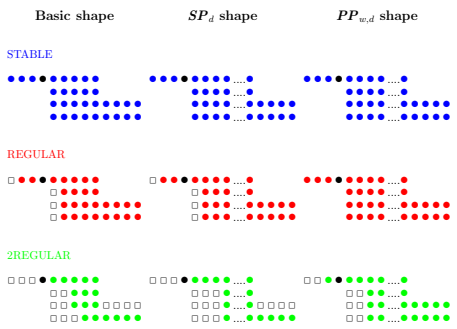
Labcd, Rabcd tie up is simple

DI: a=b, c=d, all even	**27**
SI: a=b, c=d	**223**

TIMED BM, RT ($\approx$ 2000)

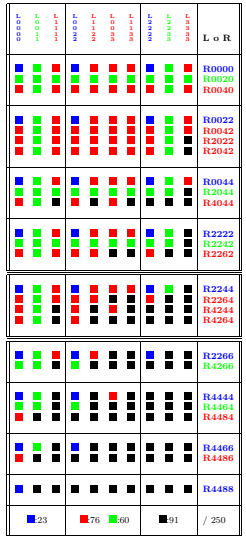
Designers are now using their insights and timing skills to cut states. Ken is world whiz on BM and RT. We can handle these protocols, but are still working on the engineering/math match up.

DI/SI Pipeline Categories



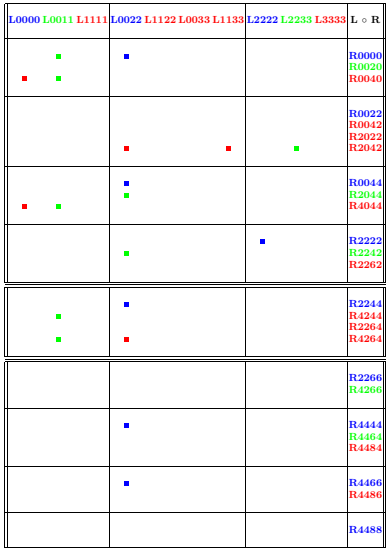
ASIDE About 2000 timed circuits are equally well behaved. The rest are toxic: stuttering, irregular, even in parallel.

DI/SI Protocol categories



NB shape preservation; capacity; pools

Published DI/SI circuit shapes



Benefits of the model

1. COMPOSITION; modal μ
2. PROPERTY CHECK shapes for 2/4phase and the persistence of cut properties (use of traces)
3. CUTAWAY STATES to generate families
4. HIDE TRACES: compose into single and parallel pipelines
5. CAPACITY patterns: retain only *capt/pass*
6. SHAPE OPTIONS: Use CCS equivalence to turn the readable spec into one more suited to the implementation

   (L | INNARDS | R)

   Systematically reveals all (9?) options per shape, each with the same pipelined behaviour.

Summary

1. The cooperation has been between a circuit wizard (Ken) and someone who isn't (me). Our results would not have happened without the both of us.
2. The mathematics has yielded: shape abstractions, relating designs via cut lattices, complete design spaces, prediction of behaviours, ... and more?
3. Ken has implemented all the live DI++SI shapes via CCS: hot from the press, reults coming soon.
4. Match between cuts and timed electrical properties
5. Applications to mixed pipelines and other hardware
6. ?Real proofs of various properties: persistence of cut properties, homogeneous parallel pipes are always independent of w... (333,333,331 Thm)