Applications of Theorem Proving to Assertion Based Verification

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PART 1: Previous Research Track Record

Mike Gordon leads the Hardware Verification Group (HVG) at the University of Cambridge Computer Laboratory. HVG has been in existence since the early 1980s and members have worked on a wide variety of formal specification and verification problems ranging from low level hardware modelling to the analysis of mixed hardware software systems. A strong theme has been experiments in semantically embedding programming and hardware description languages in logic, and then applying theorem proving. Languages that have been studied are C, Silage, ELLA, VHDL, Verilog and Handel. The tool used for this work is the HOL system, which was initially developed at Cambridge by Gordon, Melham and others. The current version is HOL4, which is now a thriving open source project hosted by SourceForge.¹

Ex members of HVG include past and present faculty at universities in the UK, Australia, Italy, North America and Hong Kong, researchers in government facilities in France, the USA and Australia and technical staff of several international companies (including Compaq, Hewlett Packard, IBM, Intel, Lucent, Texas Instruments).

The research in this proposal builds on methodological expertise gained from the successful Prosper EU project² to build electronic design automation tools ‘with theorem proving inside’. It will directly exploit and expand recent research by Gordon at Cambridge on applying theorem proving to the formal semantics of the PSL/Sugar property language.³ This work is acknowledged in the PSL Reference Manual⁴ from Accellera, and by an IBM Faculty Award to Mike Gordon.

¹http://sourceforge.net/projects/hol/
²http://www.dcs.gla.ac.uk/prosper/
³http://www.cl.cam.ac.uk/users/mjcg/Sugar/
⁴http://www.eda.org/efv/docs/psl_lrm-1.01.pdf