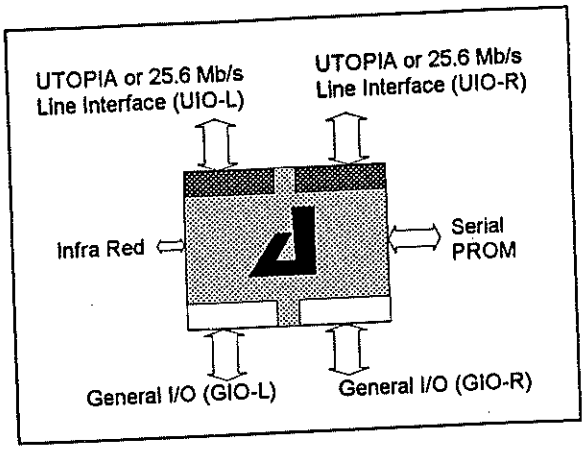
Single Chip ATM Solution
AToM-100
Preliminary DRAFT 0.3



The AToM-100 is a CMOS VLSI incorporating an ARM 32-bit RISC processor core for embedded ATM controller applications.

The device features 4 independent multiple independent IO ports of two different types (GIO and UIO), all of which support optimised ATM cell transfer under DMA.

An on-chip DRAM controller supports access to external DRAM chips without any glue logic.

Also available is a duplex infra-red port which supports standard infra-red protocols.

The RISC processor operates at 20 to 30 MHz out of internal static RAM memory or external memory. Both internal and external memory may be feely configured to serve as storage for program code, ATM cells or other data.

Some examples of the application of an AToM-100 chip are:

- Inexpensive Network Interface Card
- 2 port line card for an ATM switch
- Low cost 4 port ATM switch
- ATM access and converter for CATV set-top-box
- OEM device for digital hi-fi and audio-visual products

Features:

- CMOS Technology
- Standalone 4 port switch
- 2 ATM interfaces supporting UTOPIA
- On-chip scramblers and codec for 25.6 Mb/s ATM line code
- 2 GIO general purpose multi-format I/O ports
- Infra-red duplex I/O port
- Daisy-chain facility
- 32-bit ARM processor core
- ANSI CRC-32 coprocessor
- 16kbytes on-chip SRAM
- Initial program load from external serial ROM/EPROM
- Multichannel DMA controller
- Up to 8 simultaneous DMA operations onto on-chip RAM
- Processor core bus bond-out option

Target Applications

For a PC controller card, one of the Utopia ports is used for connection to the network hub, whereas the other is available for port sharing with another PC in a daisy chain, or for connection of local peripherals, such as a direct ATM video camera.

One GIO port is configured as a slave access port for the PC processor and is connected through appropriate buffers to the PC host bus. The other GIO is typically used for access to the internal ARM processor for connection of additional RAM or ROM or other onboard IO devices.

The figure below shows how the four ports of the AToM chip may be used in these configurations.

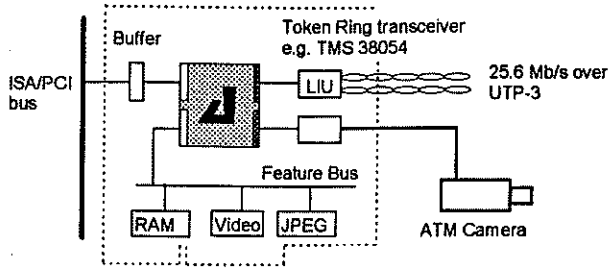
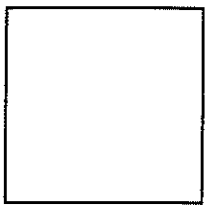


Fig. 1 - PC Network Interface Card

Set Top Box

In the set top box example, one of the Utopia ports is used for the kerbside link in conjunction with an external LIU for ADSL or CAP. The other Utopia port provides the undedicated RJ-45 ATM desktop port which can be used for additional ATM peripherals in the home. The onchip ARM processor needs be the only processor within the STB, The AToM DMA system provides data from AToM memory to MPEG decoder devices without processor overhead.



Low cost ATM switches

For a four to sixteen port ATM switch, one AToM-100 device is used per two ports. These two ports are provided by equiping the Utopia ports of the AToM-100 with appropriate LIU devices. The GIO pins are used to construct an ATM ring, with each AToM-100 offering one GIO as a bus slave to the previous device, and bonding out its processor bus on the other GIO, to be master for the next device. Standard bus devices, such as SCSI and PCMCIA ports are easily added to any of the GIO bus segments, through addition of appropriate software on the processor which is master of that bus segment.

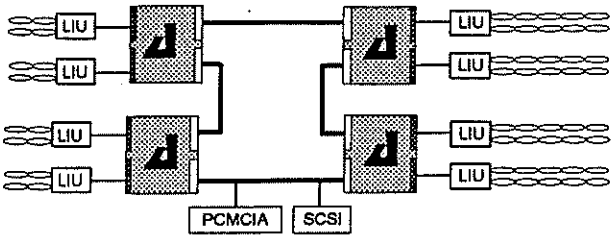


Fig. 3 - 8 port ATM switch

General ATM Module

An AToM-100 device forms the heart of a general pusrpose ATM module device. A typical configuration requires the following components:

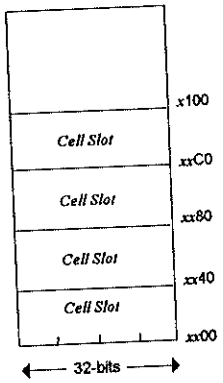
- 1 AToM-100 controller,
- 2 UTP LIU buffers and magnetics modules,
- 1 application specific codec or circuitry.

A hi-fi DAC is an example of an *application codec*. In many applications, very few additional components are required due to the programmable feature of the generic IO (GIO) port. For instance, keypads, PC parallel ports and LCD panels with integrated electronics require no additional logic, and standards such as MIDI, RS232 and audio SDIF require only simple tranceivers and opto-isolators.

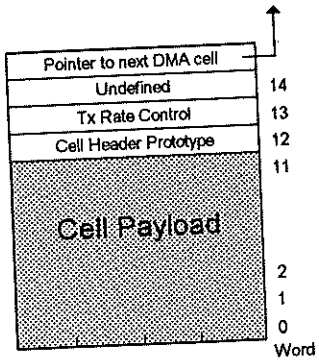
Cell-oriented direct memory access

Each of the four major ports of the AToM-100 has an identical duplex DMA controller which is able to move data to and from the main memory without processor intervention. If GIO-R is used as processor bond-out, then data can be moved from the remaining three ports to external memory on the bond-out bus in the same way as it can be moved to internal RAM, but there may be wait state penalties, depending on the external RAM speed.

The DMA hardware is optimised for 48 byte payload ATM cells. The payload of each cell is always stored on fixed boundaries in processor address space, starting with an address where the low six bits are zero. This partitions memory space into sections of sixteen 32-bit words termed *cell slots*. The first twelve 32-bit words of the section contain the cell payload, and the 12th word contains a cell header prototype. The 13th word contains rate control information for transmit cell pacing. The 15th word is a link field to the next cell slot for DMA. A null field terminates the DMA chain. The cell header error check is always stripped or added as the cell enters or exits the device.



Each DMA section/channel has a set of registers, including head pointers for transmit and receive cell slot chains, a control register, a status register and a reception VCI or VPI mask register (which provides filtering for selective reception of cells).



On any of the ports, the copying of cell headers may be disabled. This enables non-ATM devices to be connected. For instance, an MPEG decoder can be connected directly. However, data is always handled internally in cell slots. This causes most of the effort of segmentation and reassembly to happen automatically.

Chains of cells can be moved from one IO port to another simply by rewriting chain head pointers.

The Payload Type (PT) congestion indication flag of cells may be handled in hardware. The congestion indication flag of received cells is always logged in the channel section status register. For transmitted cells, the prototype from the channel slot may be selectively overwritten depending on a value in the control register.

The rate control word of each cell gives a count in quarter microseconds that the DMA channel should wait before chaining to the next cell in the queue of waiting cells and a delay before asserting end-of-chain interrupt to the ARM processor when the last cell of the queue is handled (chain field is null). This enables the processor to schedule cell transmission with fine-grain felicity and low overhead.

ARM processor

The AToM-100 chip features an on-chip Advanced Risc Machines (ARM) microprocessor core. The processor runs in its A32 D32 mode. The ARM processor is a 32 bit RISC CPU which uses 33494 transistors. The one micron, five volt implementation uses 11 square millimetres and offers 0.4 MIPS/mA at 25 MHz. The 0.8 micron and 0.5 micron implementations will be 7 mm^2 and 2.8 mm^2 respectively.

AAL-5 CRC-32 coprocessor

The AToM-100 contains a single AAL-5 CRC generator unit. The programming view of this device is a single 32 bit register, which may be freely read or written at any time, and a shadow of the whole address space of the system (invoked when address line A22 is asserted). Any processor data cycle to the shadow (read or write) will have, in addition to its normal effect, the side effect of updating the contents of the CRC32 register. In this way, the processor can cheaply calculate the CRC of any block of data that it copies or scans.

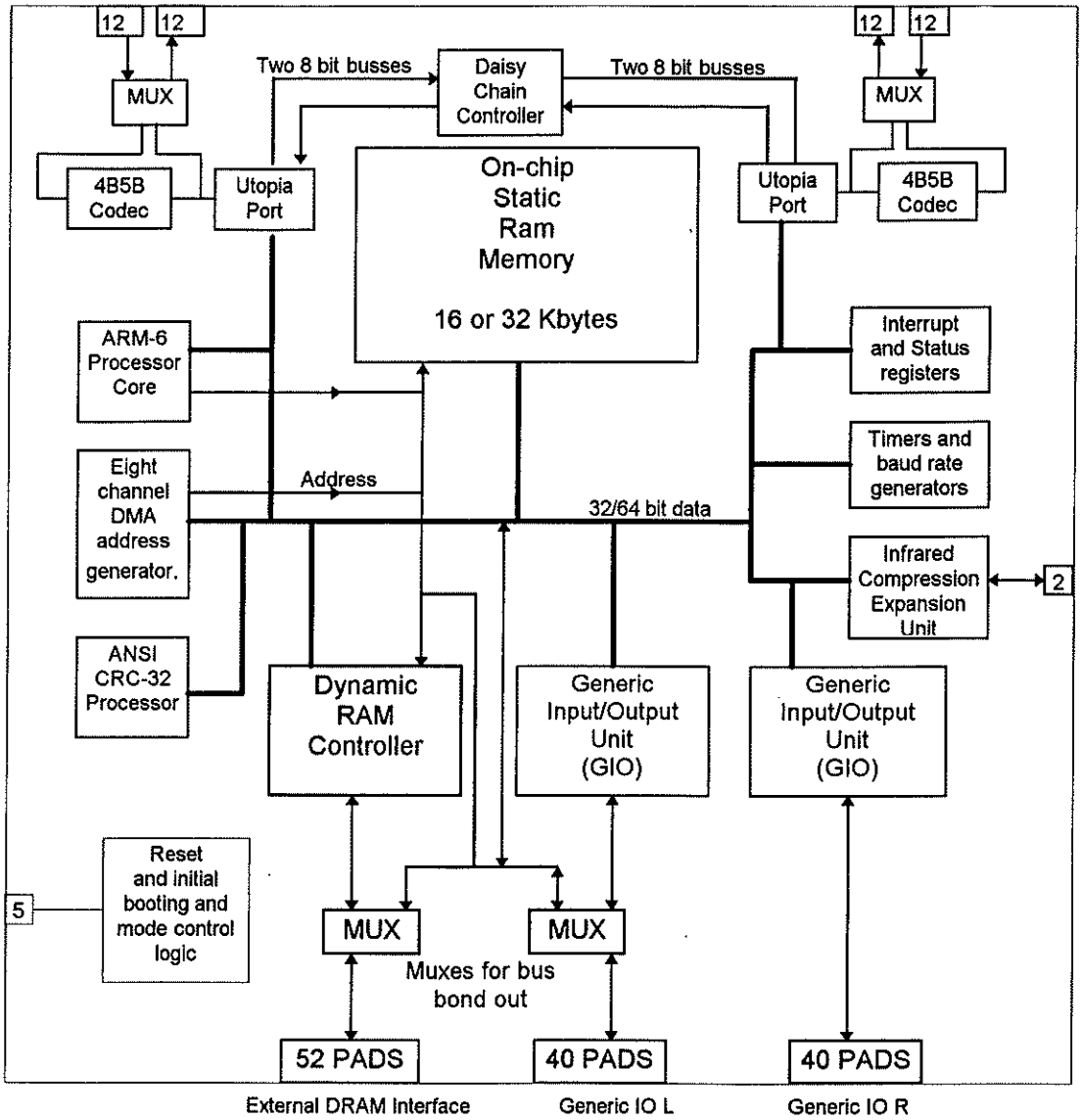


Fig. 1 AToM Chip Internal Structure

Utopia/4B5B ATM interfaces

The Utopia/4B5B ATM interfaces have two modes of operating, one as an 8-bit Utopia connection. UTOPIA (Universal Test & Operations PHY Interface for ATM) is defined asymmetrically between an ATM SAR master (i.e. switch or host logic) and a PHY slave (i.e. line interface).

For the AToM-100, the following wires are used:

- Transmit Data 0 to 7 (output).
- Transmit Start of Cell (output).
- Transmit Enable (output *).
- Transmit Clock (input/output).
- Transmit Space Available (input *).

- Receive Data 0 to 7 (input).
- Receive Start of Cell (input).
- Receive Enable (output *).
- Receive Space Available (input *)
- Receive Clock (input/output).

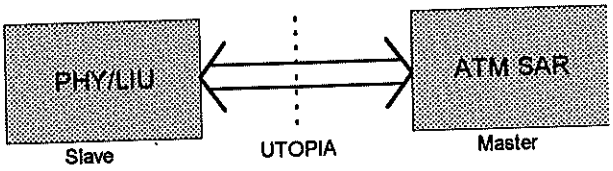
Note that the clock pins may be freely selected as outputs or inputs without modifying the specifcation of the other signals. As outputs, they are driven at half the ARM core clock, but higher frequency operation is possible when using them as inputs from an external clock.

The direction of certain of the wires may be reversed between input and output, as indicated by the asterisk. This reverses the polarity of the whole Utopia port and turns the AToM from a Utopia SAR to a Utopia PHY, allowing direct parallel daisy chaining and back-to-back operation.

In the 4B5B mode where an internal 4B5B line code is implemented. A subset of the same bond pads then take on the following functions:

- Serial data in
- Serial data out
- Serial data out inverted
- Serial clock in (32 MHz)
- Serial clock out (32 Mhz)
- Ready (PLL in lock input)
- RX LED (drive to LED indicator)
- TX LED
- LINKOK LED
- Frequency acquire (request to lock external PLL to 32 MHz reference).

The remaining pins take become general purpose user programmable IO with a data and data direction registers.



Daisy chain operation

In daisy chain mode, the two Utopia/4B5B ports are coupled internally to enable the hardware pass-on of cells and a simple multi-access protocol FSM is invoked. Cells received on one Utopia/4B5B port are transmitted on the other. The FSM generates a stream of empty cells on the transmit side of a Utopia port if the associated receive side (on the other Utpoia interface) is malframed.

In daisy chain mode, the transmit clock of each Utopia/4B5B port must be externally connected to the receive clock of the other. (This typically causes clock regeneration chains to occur, but these can be prevented by imposing FIFO stores in the external LIU devices if desired.)

The device at the ends of a daisy chain (such as at an ATM switch) should not run in the full daisy chain mode; so that the two Utopia ports of the device can be the head-ends of separate daisy chains. However they should have their multi-access FSM enabled to generate a stream of empty cell slots (header all zeros) to frame the daisy chain.

Cells passing on either bus, destined for other devices in the chain, can be ignored by a particular device through programming the reception mask register of each port (described in the section 'Cell-oriented DMA'). This enables each AtoM device on a chain to have access to a share of the VCPI space of the bus segment. Cells destined for other devices in the chain are simply passed on in hardware with no ARM processing required in the intermediate nodes.

In daisy chain mode, cells are only transmitted onto a bus if the cell slot which it overwrites previously had VCPI zero.

Generic IO units

The Generic Input Output units each support 32 data wires and 8 control wires, but these may be split into two 16 bit data groups with separate configuration. The configuration of each GIO is independent and the sub-configuration of a 16 bit subgroup is independent within a GIO. When the 16 bit subgroups are used, duplex operation is possible, with one subgroup (eg GD0-GD15) being used for input and the other for output. In particular, 16 bit Utopia is supported on the FIO ports. 8 bit Utopia is also supported, where the unused 8 signals of each direction become independent, additional PIO (programmable input or output).

GIO modes are selected in the GIO configuration register of each GIO, from among the following modes:

- PIO mode
- FIFO mode
- Processor bond-out mode (GIO-R only).

In PIO mode, the processor accesses the GIO using programmed IO to a readable and writeable volatile register. The flags in this register are routed to the AToM-100 pads using the programmable logic described in the next section.

In FIFO mode, the GIO DMA controller is enabled and autonomous transfer of data from and to the GIO is possible. The DMA unit is identical to those used for the Utopia ports and has the same internal cell-oriented structure, but the external device need not know anything about the internal ATM representation of the data.

However, for ATM devices connected to a GIO, this facility can be helpful. In FIFO mode, the external device can simply be the bus of another processor, such as the host CPU in a Network Interface card, or the bond-out of another AToM-100 which is running asynchronously. In this latter case, data can be transferred to and from the AToM-100 device using programmed IO cycles on the external processor which map into DMA cycles to the internal address space.

Programmable logic

Each GIO is isolated from the bond pads which are available to it by a section of programmable logic. This logic is programmable in software from the ARM core. The logic can be used to create simple physical layer protocols and provides flexibility in the interrupt conditions for the GIO. Both serial and parallel data transfer can be implemented. Specific parallel forms are PC parallel port and Utopia. Serial protocols include RS232 (and MIDI) and the SDIF Manchester coding used for digital hifi. Each half of a UIO contains sufficient logic for both a duplex RS232 and SDIF serialiser at once.

Duplex Infra Red Interface

The infra red interface consists of a transmit and a receive port. Both ports consist of a single CMOS compatible pin. The transmit port requries an external power MOS-FET and an IR transmit diode. The receive port requires an external photodetector and a pulse conditioner with AGC. Only line codes which are pulse density modulated are supported (which is all known line codes) and a fixed transmit pulse of 1.8 microseconds is provided (although this can be altered with an external mono-stable if required).

The processor interface to the IR port is through a symmetric compression-decompression unit which performs loss-less run-length compression. The processor interchanges 32 bit words with the IR port under interrupt control. The 32 bit word contains three packed count fields:

- Number of pulses,
- Spacing of pulses (in quarter microseconds),
- Interval after last pulse in run (in quarter microsconds).

Because the compression is lossless, any IR physical line code can be implemented in software.

Initial program load

Initial program load from external serial ROM/EPROM is supported. Two pins are used: IPLD and IPLCK (which actually doubles as the AK pin of GIO-B). If IPLD is high while processor reset is asserted (and for the first clock cycle after), then the AToM-100 will generate a clock on IPLCK which can be used to clock data out of an external serial ROM/EPROM. After a preamble pattern is recognised, data will be placed in sequential bits of the onboard RAM. After 65536

bytes worth of data have been clocked (only the leading data need form a valid program), the processor reset will be deasserted.

If IPLD is low during reset, the ARM processor core bond out is enabled and the ARM will execute its standard reset sequence directly after deassertion of reset.

Package

The AToM-100 is available in 144 pin quad flat pack. The five volt 0.8 micron implementation with 32 Kbytes of static RAM is estimated to have a die size of 7 millimetres square and a power consumption of 1.5 watts.

User Programmable ATOM register resources (preliminary)

Number of copies	Register Name	Size and mode
8	CSSR = channel section status register. Provides status for a direction of an Atom DMA channel	R/W 31:16
8	CSCR = channel section control register. Provides configuration for a direction of an Atom DMA channel	R/W 31:16
8	IOCR = Input/output configuration register. Provdes configuration of a GIO or UIO port	R/W 15:0
8	CSAR = channel section address register. Provides the DMA slot pointer for a direction of an Atom DMA channel	R/W 31:6
8	IOSR = Input/output status register. Provides status and error flags for a GIO or UIO port	R/W 15:0
2	GIOD = Generic Input / Output Data Register. Used in PIO mode for software input and output. Also used for access to the asynchronous and PDIF UART macros, etc.	R/W 31:0
2	GIODDR = Generic Input / Output Data Direction Register.	R/W 31:0
1	MCR = master control register. Provides refresh and Interrupt enables and memory map configuration	R/W 31:0
1	MSR = master status register. Provides Interrupt and configration status	R/W 31:0
1	IRCR = infra red control register	R/W 4:0
1	IRSR = infra red status register	R/W 4:0
1	IRRX = IR rx data register	R/O 31:0
1	IRTX = IR tx data register (w/o)	W/O 31:0
4	VPCM0 = VCI VPI Mask 0 register. Cell header bit aask register for selective received cell filtering	R/W 27:4
4	VPCM1 = Match register for received cell filtering	R/W 27:4
1	CRCREG = CRC-32 (AAL-5 register)	R/W 31:0
1	ACR = DMA control register. Provdes priority allocation and master enables for DMA.	R/W 31:0
4	CTCR = Counter timer control register	R/W 7:0
4	CSCR = Counter timer status register	R/W 7:0
4	CTCR = Counter timer count register	R/W 31:0
4	CTCHR = Counter timer capture/hold register	R/W 31:0

Note: Bit assignments within the registers and programming information will be given in the final version of this data sheet.

Application Note

Modes of AToM chip parallel interconnection.

AToM devices may be interconnected in quite a variety of ways, including in various forms of daisy chain and on host or multi-access busses. Clearly they can be connected using their serial 4B5B links, and this can be done in both daisychain mode and as autonomous ATM links (i.e. standard ATM links). In this application note, we concentrate on parallel bus interconnection of AToMs.

Processor Bus Parallel Interconnection

The GIO port of an AToM device may be connected as a slave device to the bus of another processor, which could, infact, be another AToM device operating in bus bond-out mode. There may be any number of such AToM slaves on a bus, and they can be individually addressed either by selective strobing using master processor address bus decoding, or by running their GIO port in ATM mode (cell headers on) and using the cell recpetion mask registers within the AToM

Back-to-Back Mode

In back-to-back mode, we can connect two AToM devices to each other on their Utopia ports. This can be done

1. With hardware flow control (i.e. wiring the cell available /cell space available signals to each other)
2. Without hardware flow control (i.e. leaving the flow control wires open)
3. In daisy chain mode (where flow control does not apply since rates are fixed)

In all three configurations, the clock wires may be driven from any sensible source (including a third party external source) without considerable consideration.

For the with-flow control mode, we typically make the output side the of the AToM chip behave as a Utopia SAR and the input side as a Utopia PHY.

For the without-flow control mode, the available pins are programmed as outputs and not connected to each other (ie left open). This gives the same flow and discard semantics as a 4B5B or other ATM link.

In daisy chain mode, all clock inputs for one direction of the daisy chain must come from a common clock source since elastic buffering within the daisy chain is not supported by AToM (although there is some).

Utopia Backplane Bus with Multi-access mode.

In a rack with a backplane, AToM chips may be situated one or two (or more) per plug-in card and there may be empty slots in the rack.

In this case we do not wish the data to be daisy chained through the AToM chips, since reliability and unfilled rack slots are issues. Instead a shared backplane bus switch can be created, similar to the ATM Multiphy standard for Utopia, but without using additional pins (which are unavailable).

This application note suggests a true ATM bus solution for the case where the bus has one card which is the master (which could also contain an AToM) and which originates most of the data received by the AToM-based line cards. The proposal can be modified to use a single bus without a unique master, but at half the throughput. With the dual bus, all data sent from the AToM cards is received only by the master, and vice versa, so we have no direct peer-to-peer comms between the line cards.

Two 9 bit busses are used, one for receive and one for transmit. Each bus has the following nets: an eight bit data bus and a start oc cell line (SOC).

Clock distribution is required in an appropriate form, providing a free-running clock for each bus, although these two clocks can be common. The maximum clock speed will probably be determined by the bus skew, and will be typically 5 to 25 MHz.

For RECEIVE (from the master to the slave card)

By receive we mean data being sent from the bus master to the line cards. This is easily achieved by configuring the receive UIO ports of the AToMs as PHY devices and wiring their Utopia input pins to the common receive bus. Selection of cells by a particular line card is achived by using the VCI ond VPI mask registers in each AToM chip. Cells with undesired VCI/VPIs are simply dropped in the internal AToM Utopia interface. The RXAV signals from each AToM should be left open and ignored. Note that multicast is achieved.

For TRANSMIT (to the master of a backchannel from the slaves).

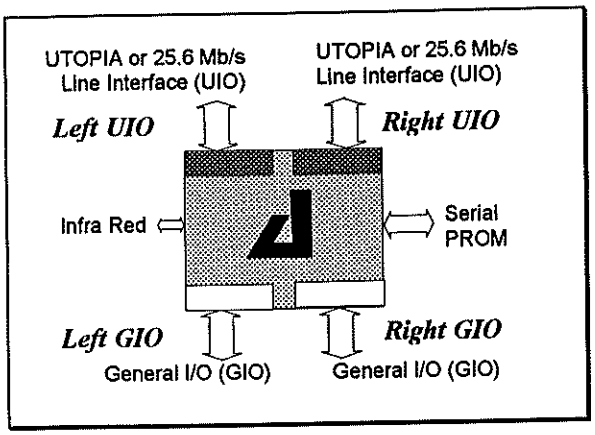
Arbitration is required to prevent cell collisions and to enable only one AToM chip to drive the transmit bus.

To avoid daisychaining of a token passing wire, each slot uses a pair of separate wires back to an arbitrator. The transmit ports of the UIOs are also run in PHY mode, but modified through a configuration bit in their CSCR to assert TXAV as a request to send and use TXEN as a grant. These form the two wires per AToM device (or card through additional oncard arbitration logic). The TXEN signal is both an acknowledge and an output enable for the rxsoc and rxdata bussed wires.

The arbiter should assert TXEN to one device at a time and for whole cell intervals. A cell interval may be determined by the arbiter by dividing the clock by 53 and resetting its counter on valid SOC cycles.

Note: the AToM chip utopia data outputs have limited drive strength and external tri-state bus drivers must be used if a large bus load is planned.

Pin Functions



UIO Signals (24 pins)

8-bit UTOPIA mode

Signal Name	Pins	Type	Description
P_ul_rx_data	0:7	In	Received Data
P_ul_rx_ck		InOut	Rx Clock
P_ul_rx_soc		In	Rx Start of Cell
P_ul_tx_enb		In	Rx Enable
P_ul_rx_av		InOut	AToM is ready output
P_ul_tx_data	0:7	Out	Transmit Data
P_ul_tx_ck		InOut	Tx Clock
P_ul_tx_soc		Out	Tx Start of Cell
P_ul_rx_enb		InOut	Tx Enable
P_ul_tx_av		InOut	LIU is ready input

4B5B mode

Signal Name	Pins	Type	Description
P_ul_rxdata		In	Receive Serial Data stream
P_ul_redyb		In	LIU PLL is ready
P_ul_rx_pio	0:5	In	Programmable I/O input
P_ul_rx_led		Out	Cell Received
P_ul_rx_happy		Out	High when a cell is received without error. Low for errored cells or REDYB is deasserted or line violation detected
P_ul_rx_ck		InOut	Rx Clock (32 MHz)
P_ul_tx_txdata		Out	Transmit Serial Data stream
P_ul_tx_txdata*		Out	Inverted Tx Serial Data stream
P_ul_tx_pio	0:5	Out	Programmable I/O output
P_ul_tx_led		Out	Cell Transmitted
P_ul_tx_ck		InOut	Tx Clock (32 MHz)
P_ul_tx_fraq		Out	Frequency Acquire

2 pins unused

Left or Right GIO Signals - 40 pins

16-bit Duplex UTOPIA mode

Signal Name	Pins	Type	Description
P_gl_rx_data	0:15	In	Received Data
P_gl_rx_ck		InOut	Rx Clock
P_gl_rx_soc		In	Rx Start of Cell
P_gl_tx_enb		In	Rx Enable
P_gl_rx_av		InOut	AToM is ready output
P_gl_tx_data	0:15	Out	Transmit Data
P_gl_tx_ck		InOut	Tx Clock
P_gl_tx_soc		Out	Tx Start of Cell
P_gl_rx_enb		InOut	Tx Enable
P_gl_tx_av		InOut	LIU is ready input

In 8-bit mode, there is no change except that the data wires from d8 to d15 are not used and twice as many cycles are needed per cell. Pins d8 to d15 revert to PIO mode and may be used freely.

Left or Right GIO signals.

32 bit half-duplex FIFO mode

Signal Name	Pins	Type	Description
P_glr_txok		Out	TX space available
P_glr_rxok		Out	RX space available
P_glr_soc		In Out	Tag bit
P_glr_data	31:0	InOut	Data transfer Bus
P_glr_rwbar		In	Read or write direction
P_glr_strobe		In	Strobe

In 32 bit half-duplex mode, data may be read or written by the external processor or controller to cause DMA into internal AToM memory map.

Further modes of the GIO supported by the programmable logic will be added in the final version of this data sheet.

The bus bond out pin assignment will be added in the final version of this data sheet.

DRAM Controller Signals - 48 pins

Signal Name	Pins	Type	Description	
P_dramdata	0:31	InOut	32-bit DRAM data bus	
P_casb		0:3	Out	CAS strobes
P_rasb			Out	RAS strobe
P_webar			Out	Write enable
P_muxabus	0:9	Out	Multiplexed RAM address bus	

Miscellaneous Signals - 5 pins

Signal Name	Pins	Type	Description	
P_ir_input		In	Infra-red input	
P_ir_output		Out	Infra-red output	
P_resetb			In	Active low reset input
P_busclk		In	ARM processor clock input	
P_ipld			In	Mode and Boot input

The operating modes of the AToM are chosen during the boot process - serial input - describe....

Timing Digrams

... Timing description & diagrams