

COMPUTER SCIENCE TRIPOS Part IB – 2020 – Paper 5

1 Computer Design (swm11)

- (a) What is Moore's law for CMOS technology scaling? [3 marks]
- (b) Why does the performance of wires not scale with transistor technology shrinks? [3 marks]
- (c) What determines the maximum clock frequency that a digital circuit can be safely clocked at? [3 marks]
- (d) In SystemVerilog, when is a variable of type `logic` implemented as a `wire` rather than a `reg`? [3 marks]
- (e) Consider the following three correct implementations of the function `fib` that compute the Fibonacci sequence.

```
module fibA(input          clk,
            input          rst,
            input logic [5:0] n,
            input logic    start,
            output logic [20:0] r);

function automatic longint fibr(longint n);
    fibr = (n<2) ? n : fibr(n-1) + fibr(n-2);
endfunction

always @(posedge clk or posedge rst)
    if(rst)
        r <= 0;
    else
        if(start)
            r <= fibr(n);
endmodule

module fibB(input          clk,
            input          rst,
            input logic [5:0] n,
            input logic    start,
            output logic [20:0] r,
            output logic    busy);

logic [20:0] a,b;
logic [ 5:0] j;
always @(posedge clk or posedge rst)
    if(rst)
        {busy, r, a, b} <= 0;
    else
        if(start)
            {busy, r, a, b, j} <=
                {1'd1, 21'd0, 21'd1, 21'd0, n};
        else
            if(j!=0) begin
                a <= a+b;
                b <= a;
                j <= j-1;
            end
            else {busy, r} <= {1'd0, b};
endmodule

module fibC(input          clk,
            input          rst,
            input logic [5:0] n,
            input logic    start,
            output logic [20:0] r);

// initialise ROM
logic [20:0] fibrom [0:31] =
    { 0, 1, 1, 2,
      3, 5, 8, 13,
      21, 34, 55, 89,
      144, 233, 377, 610,
      987, 1597, 2584, 4181,
      6765, 10946, 17711, 28657,
      46368, 75025, 121393, 196418,
      317811, 514229, 832040, 1346269};

always @(posedge clk or posedge rst)
    if(rst)
        r <= 0;
    else if(start) r <= fibrom[n];
endmodule
```

- (i) How many clock cycles does it take for each module to compute $fib(8)$ in simulation? Justify your answer. [6 marks]
- (ii) Which of these modules is synthesisable? Justify your answer. [2 marks]