COMPUTER SCIENCE TRIPOS Part IA – 2019 – Paper 2

2 Digital Electronics (ijw24)

(*a*) (*i*) Briefly describe the ways in which sequential logic differs from combinational logic.

[2 marks]

(*ii*) Describe the main features that differentiate synchronous from asynchronous sequential logic.

[4 marks]

(*b*) A synchronous 3-bit counter implemented using D-type Flip-Flops has a mode control input M. When $M = 0$, the counter output sequence represented in decimal form is 0, 1, 2, 3, 4, 5, 6, 7, and repeat. When $M = 1$, the counter output sequence represented in decimal form is 0, 1, 3, 2, 6, 7, 5, 4, and repeat. The Flip-Flop outputs are $\{Z_2 Z_1 Z_0\}$ where Z_0 represents the least significant bit of the counter output.

(*i*) Draw a state diagram that describes this counter.

[4 marks]

(*ii*) Write down the state transition table corresponding with the state diagram in Part (*b*)(*i*).

[2 marks]

(*iii*) Determine the excitation combinational logic in sum of products form for D-type Flip-Flop input D_0, i.e., the input of the Flip-Flop that represents the least significant bit of the counter. Show that the required combinational logic can be implemented using a 2-input XNOR gate plus some other combinational logic gates.

[3 marks]

(*c*) Use row matching to reduce the number of states required to represent the single input (X), single output (Z), Mealy finite state machine described in the following state transition table:

Current State	Next State		Output (Z)	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
A	B	C	1	0
B	F	D	0	0
C	D	E	1	1
D	F	E	0	1
E	A	D	0	0
F	B	C	1	0

Draw the resulting state diagram. [5 marks]