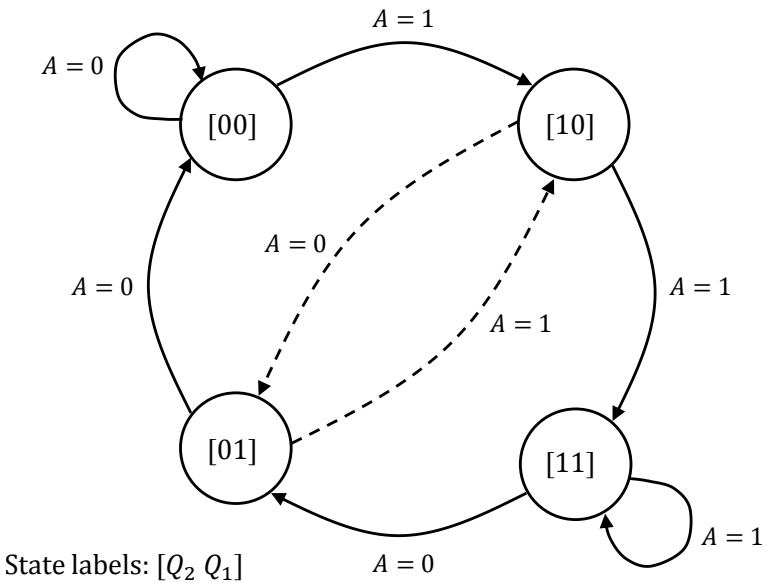
COMPUTER SCIENCE TRIPOS Part IA – 2018 – Paper 2

2 Digital Electronics (IJW)

(*a*) State the main features of a synchronous finite state machine (FSM) and describe its two main forms. [6 marks]

(*b*) With the aid of a diagram, show how a Transparent D-Latch can be implemented using cross-coupled NOR gates and some additional combinational logic. What are the advantages of the Transparent D-Latch over the RS latch? [6 marks]

(*c*) An FSM with input A has the function described in the following state diagram and is to be implemented using two synchronously clocked D-Type flip-flops as the state registers.



(*i*) Write down the corresponding state table taking into account all transitions in the state diagram, indicated by both solid and dashed lines. Show that the required FSM can be implemented by connecting the D-Type flip-flops in the form of a shift register.

(*ii*) For the implementation in Part (*c*)(*i*), what effect does increasing the clock rate of the D-Type flip-flops have on the likelihood of occurrence of the dashed-line transitions?

(*iii*) The two dashed-line transitions have the property of inverting Q_1. We now wish to replace both of them with transitions that occur under the same circumstances but instead have the property that Q_1 is unchanged. Give the four possible state diagrams satisfying this requirement and, for each state diagram, determine the next-state logic for the D-Type flip-flops.

[8 marks]