COMPUTER SCIENCE TRIPOS Part IB - 2015 - Paper 5

2 Computer Design (SWM)

- (a) What is the von Neumann bottleneck and why can it limit performance on today's RISC machines? [4 marks]
- (b) What computer architecture techniques are used to mitigate the effects of the von Neumann bottleneck on RISC machines as compared to early computers like EDSAC? [4 marks]
- (c) How do RISC machines enforce memory protection for applications with disjoint data sets? [4 marks]
- (d) What is segmented addressing (e.g. as used on x86 machines)? [4 marks]
- (e) If non-volatile random access memory had similar performance and cost to DRAM, how would this change the memory hierarchy? Justify your answer.

 [4 marks]