## COMPUTER SCIENCE TRIPOS Part IA - 2014 - Paper 2

## 2 Digital Electronics (IJW)

(a) Show how two NOR gates may be connected to form an RS latch. Describe its operation and give a table relating its inputs to its outputs. How could you use this circuit to eliminate the effect of contact bounce in a single pole double throw switch supplying an input to a digital logic circuit?
(b) The state sequence for a particular 4-bit binary up-counter is as follows:

| $Q_{A}$ | $Q_{B}$ | $Q_{C}$ | $Q_{D}$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| $\vdots$ | $\vdots$ | $\vdots$ | $\vdots$ |
| 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| $\vdots$ | $\vdots$ | $\vdots$ | $\vdots$ |

Show how four negative edge triggered T-type flip-flops (FFs) with outputs labelled $Q_{A}, Q_{B}, Q_{C}$ and $Q_{D}$ can be used to implement a ripple counter having the specified state sequence. Show any combinational logic necessary assuming that the FFs have asynchronous reset inputs available.
[4 marks]
(c) Using the principles of synchronous design, determine the next state combinational logic expressions required to implement a counter having the state sequence specified in part (b). Assume that D-type FFs are to be used and that unused states do not occur.
(d) Explain carefully what happens if the counter in (c) starts in state 1110 . In general, how can start-up problems be overcome in the design of synchronous state machines?
(e) What are the advantages and disadvantages of the synchronous design in part $(c)$ compared with the alternative design in part (b)?
[2 marks]

