COMPUTER SCIENCE TRIPOS Part II – 2013 – Paper 9

11 System-on-Chip Design (DJG)

(*a*) List a set of parallel wires that might form a parallel, synchronous interface for transferring 4-bit words when both sides are ready to communicate. [3 marks]

(*b*) Describe in words the protocol used over the interface of part (*a*). Use a timing diagram as well if helpful. [3 marks]

(*c*) Give the circuit for a receiver that is conformant to your interface and protocol from part (*a*) and part (*b*). It should simply store the received data in a register. Use Verilog-style RTL instead of a circuit diagram if you wish. [3 marks]

(*d*) Give, with justification, the maximum throughput of your protocol above in terms of words per clock cycle. [1 mark]

(*e*) A FIFO component (first-in, first-out queue) has two instances of the above interface that share a common clock. Can it be designed so that there is no combinational logic path between the two instances? What does this mean for its behaviour? [5 marks]

(*f*) A variation on the FIFO component has independent clocks for the two instances of the interface. It is used for transferring data between two clock domains. How would it be designed internally and what is its maximum throughput? [5 marks]