COMPUTER SCIENCE TRIPOS Part II – 2013 – Paper 8

13 System-on-Chip Design (DJG)

(a) Why do System-on-Chip designs use both on/off power control over subsystems
as well as adjustable supply voltages when a subsystem is switched on?

[5 marks]

(b) How might the two techniques from part (a) be used in conjunction in a server
that contains four similar processing elements that take jobs from a shared
queue? State any assumptions you make. For instance, you might assume each
processing element consists of about 50,000 gates, that job queue entries are
about a kilobyte in length and that their arrival rate varies greatly.   [5 marks]

(c) A simulation of the four processing elements that modelled each gate in
detail would be slow. Briefly describe *two* alternative simulation models that
respectively model less and far less detail, while still preserving accuracy in terms
of the job queue length variation.   [3 marks each]

(d) Would the supply voltage variation need to be modelled in each of your two
models of part (c)?   [2 marks]

(e) How can a single simulation mix a low-level model of one processing element
with a high-level model of the remainder?   [2 marks]