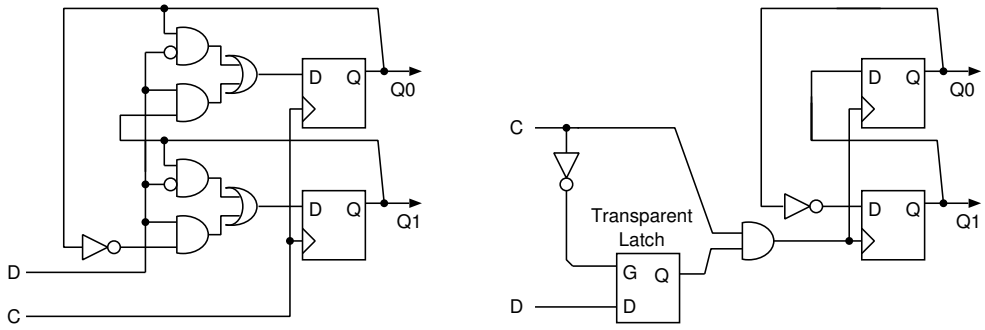
COMPUTER SCIENCE TRIPOS Part II – 2012 – Paper 9

11 System-on-Chip Design (DJG)

(*a*) Give a basic formula for modelling delay in logic circuits once wiring length is known. [2 marks]

(*b*) Give a basic formula for modelling power consumption in logic circuits once wiring length is known. [2 marks]

(*c*) The figure below gives two versions of a finite-state machine before and after a modification.



Give the name of this modification, say why is it performed and fully explain the role of the additional latch. [4 marks]

(*d*) Three power saving techniques used in current SoCs are dynamic voltage and frequency scaling (DVS), clock gating and power supply gating. Compare and contrast these three techniques in terms of

(*i*) physical granularity [3 marks]

(*ii*) temporal granularity [3 marks]

(*iii*) the manual complexity they add to the design flow [3 marks]

(*e*) Including power consumption, discuss what design considerations result in a product using an FPGA (field-programmable gate array) rather than an application-specific integrated circuit (ASIC)? [3 marks]

[*Note:* In all sections, marks will be awarded for sensible argument even if assumptions or results are incorrect.]