COMPUTER SCIENCE TRIPOS Part II – 2012 – Paper 8

13 System-on-Chip Design (DJG)

The inner loop of an application program, to be implemented within a SoC, performs a lot of bit-intensive operations on 64-bit numbers. Two of the operations are counting the number of ones and reversing the bits.

(*a*) What design considerations should be taken into account when deciding whether to speed up the implementation of these operations using custom hardware? [5 marks]

(*b*) Summarise each of the following three means of coupling general custom hardware to a processor sub-system within a SoC:

(*i*) implemented as a custom instruction [2 marks]

(*ii*) implemented in a peripheral controlled using programmed I/O [2 marks]

(*iii*) implemented in an autonomous bus master [2 marks]

(*c*) Discuss whether each of the three means of part (*b*) could be appropriate for the bit-intensive operations mentioned above. [4 marks]

(*d*) Technology predictions are that chip transistor count can continue to grow provided a lower percentage of the chip is in use at any one time. How can large parts of application programs be implemented in custom hardware and would this match technology trends? [5 marks]

[*Note:* In all sections, marks will be awarded for sensible argument even if assumptions or results are incorrect.]