**COMPUTER SCIENCE TRIPOS Part IA − 2012 − Paper 2**

1 Digital Electronics (IJW)

(a) Show how a transparent D latch can be constructed using an RS latch and some combinational logic gates. Briefly describe the operation of such a transparent D latch. [4 marks]

(b) A 3-bit synchronous counter has a mode control input X. If $X = 0$, the counter steps through the binary sequence 111, 110, 101, 100, 011, 010, 001, 000, and repeat, or if $X = 1$, the counter advances through the Grey code sequence 111, 101, 100, 000, 001, 011, 010, 110, and repeat. Draw the state diagram for the counter. [6 marks]

(c) A machine has the state diagram shown below, where N and D are two inputs and $N = D = 1$ cannot occur. The state assignment is $S_0 = [00]$, $S_1 = [01]$, $S_2 = [10]$ and $S_3 = [11]$, where the machine starts in state S_0 and finishes in state S_3. Note that state $= [Q_1 Q_0]$ where Q_n is the output of flip-flop n.
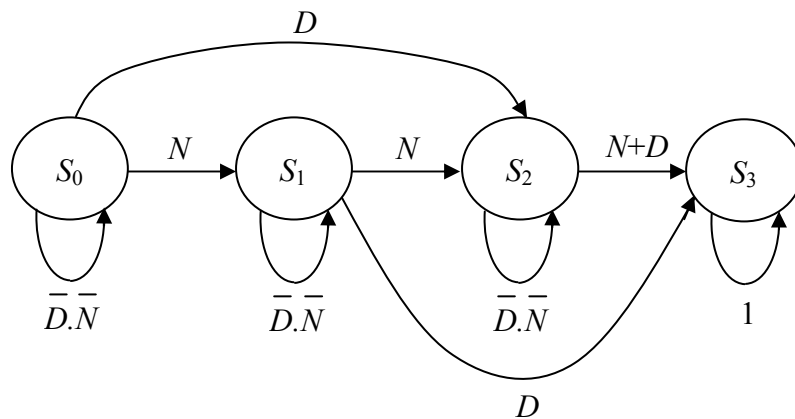
(i) Write down the state transition table for this machine. [6 marks]

(ii) Assuming the use of D-type flip-flops for the state registers, determine the minimised Boolean expressions for the next state functions. [4 marks]