COMPUTER SCIENCE TRIPOS Part IB

Wednesday 6 June 2012 1.30 to 4.30

COMPUTER SCIENCE Paper 5

*Answer **five** questions.*

*Submit the answers in five **separate** bundles, each with its own cover sheet. On each cover sheet, write the numbers of **all** attempted questions, and circle the number of the question attached.*

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

STATIONERY REQUIREMENTS
Script paper
Blue cover sheets
Tags

SPECIAL REQUIREMENTS
Approved calculator permitted

1 Computer Design

Below is a SystemVerilog module (`shaft_decoder`) and its test bench (`run_test`).

```
module shaft_decoder(
    input                clock,
    input                reset,
    input [1:0]        grey_code,
    output logic [7:0] position);

   logic   previous_code;
   always_ff @(posedge clock)
    case({previous_code, grey_code})
      4'b00_01, 4'b01_11, 4'b11_10, 4'b10_00: position <= position+1;
      4'b00_10, 4'b10_11, 4'b11_01, 4'b01_00: position <= position-1;
    endcase
endmodule


module run_test();
   logic clock;
   logic reset;
   logic [1:0] grey_code;
   logic [7:0] position;

   shaft_decoder dut(.clock, .reset, .grey_code, .position);

   initial begin
       clock = 1;
       reset = 1;
       grey_code = 2'b00;
   #10 reset = 0;
   #10 grey_code = 2'b01;
   #10 grey_code = 2'b11;
   #10 grey_code = 2'b10;
   #10 grey_code = 2'b00;
   #10 grey_code = 2'b10;
   #10 grey_code = 2'b11;
   #10 grey_code = 2'b01;
   #10 grey_code = 2'b00;
   #10 grey_code = 2'b10;
   #10 grey_code = 2'b01;
   #30 $finish;
   end

   always #5 clock = !clock;

   always @(posedge clock)
     $display("%05t: grey_code=%2b position=%03d",
              $time,grey_code,position);

endmodule
```

The `shaft_decoder` module takes a two-bit grey-code sequence from an optical shaft encoder (e.g. one of the two directions on a mechanical mouse) and outputs an 8-bit position. When the shaft is rotating in the positive direction, the following sequence of inputs is seen: $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$. The shaft is rotating in the negative direction if the reverse sequence is seen. When the shaft is not moving, the input does not change. Inputs arrive asynchronously.

(*a*) The `shaft_decoder` module is syntactically correct but functionally slightly erroneous. What are the errors? [8 marks]

(*b*) In the `run_test` module:

(*i*) At what times will clock edges be produced (in simulation time units) and when will reset be deasserted? [4 marks]

(*ii*) What will be the output sequence for `position` for the whole simulation? [4 marks]

(*c*) What are the advantages of simulation over test on reconfiguration hardware? [4 marks]

2 Computer Design

Consider the following code which takes an array `d` of `n` 32-bit integers and performs a bubble sort.

```
for(i=0; i<n; i++) {
  int m = n-i-1;
  for(j=0; j<m; j++)
    if(d[j]>d[j+1]) {
      t = d[j];
      d[j] = d[j+1];
      d[j+1] = t;
    }
}
```

(*a*) Given the following register allocation, how would the inner loop be encoded in assembler for a MIPS-32 style processor (i.e. a RISC machine with a load-store architecture and conditional branches being the only conditional instruction)? Assume that there are no delayed branches (unlike MIPS-32), do not unfold the loop and please do comment your code.

register	variable	description
r4	`d`	base address of array d
r5	`m`	value of m
r6	`j`	register used to hold j
r7	`t`	register to hold temporary t

[8 marks]

(*b*) The classic 32-bit ARM instruction set makes every instruction conditional. How can your code make use of conditional instructions to reduce the number of data-dependent branches? [5 marks]

(*c*) Given the classic 5-stage pipeline (below), how do the control and data hazards differ between your code in parts (*a*) and (*b*)? What is the impact on performance? [7 marks]

instruction fetch	branch, decode & register read	execute	memory access	write back

3 Computer Design

(*a*) What are the differences and similarities between a branch, a software exception (SYSCALL on MIPS, SWI on ARM), an exception and an interrupt? [6 marks]

(*b*) What is the difference between precise and imprecise exceptions? [4 marks]

(*c*) What does a TLB do and how does it do it? [5 marks]

(*d*) TLB misses can be handled in hardware or software. If misses are handled purely in software, how are they made transparent to the user code? [5 marks]

4 Computer Networking

(*a*) In a data-center context, describe a *straggler* using two examples. [2 marks]

(*b*) (*i*) Describe the *TCP incast* problem. [2 marks]

(*ii*) Outline and critique a solution to the *TCP incast* problem. [3 marks]

(*c*) (*i*) Show that to achieve a steady-state throughput of 10 Gbps, a TCP session with a Round-Trip-Time (RTT) of 100 ms and a Maximum-Segment-Size (MSS) of 1500 bytes can tolerate a packet loss probability of less than 2×10^{-10}. [4 marks]

(*ii*) Compute the potential packet-memory requirement of either end-system implementing Selective-Acknowledgements (SACK). [3 marks]

(*iii*) What is the tolerable packet loss probability if this same network (same MSS and RTT) operated at 100 Gbps? [2 marks]

(*d*) Some experts say: *"Many TCP transactions in the Internet never enter congestion-avoidance."* Discuss this claim.
[*Hint:* It has been measured that greater than 90% of web objects are less than 10 Kbytes.] [4 marks]

5 Computer Networking

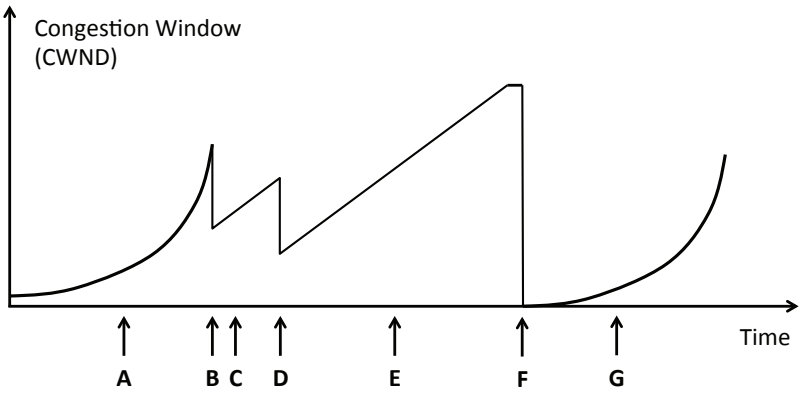
(*a*) (*i*) Define the terms *capacity* and *latency* as applied to communication channels; explaining whether there is a **strict** relationship between the capacity of a channel and its latency. [3 marks]

(*ii*) Using a clear example explain how the latency of a channel can have a direct effect on the capacity of a higher-layer channel which uses it. [8 marks]

(*iii*) Describe how the capacity of the higher-layer channel may be improved, without any change to the characteristics of the underlying channel. [3 marks]

(*iv*) Describe in what circumstances such changes would provide only limited benefit. [2 marks]

(*b*) The figure below illustrates, for a single TCP connection, changes in the advertised congestion window (CWND).



(*i*) Indicate which phase of congestion control the TCP connection is in at **G**.

(*ii*) Indicate which phase of congestion control the TCP connection is in at **E**.

(*iii*) Describe the event that has occurred at **D**.

(*iv*) Describe the event that has occurred at **F**.

[1 mark each]

6 Computer Networking

(*a*) Consider the host `mine.ja.net`, with a local DNS server `dns1.ja.net`. [*Note:* `dns1.ja.net` is configured to use recursive DNS by default.]

(*i*) Host `mine.ja.net` asks server `dns1.ja.net` to resolve the hostname `yours.foobar.com`. Assume there are no cached entries relevant to this request. Write down the steps taken to resolve `yours.foobar.com` and respond to `mine.ja.net`. [4 marks]

(*ii*) Describe the differences between this solution and one achieved using iterative DNS. [2 marks]

(*iii*) Compare and contrast DNS with ARP. [4 marks]

(*b*) An office has an (Internet) access link rated at 10 Mbps full-duplex. Each user requires 1 Mbps when transmitting and each user is active 10% of the time.

(*i*) Initially a static allocation of bandwidth is made for each user. How many users can the access link support? [1 mark]

(*ii*) The office opts for a pure packet-switched access link. What is the probability that a given user is transmitting? [1 mark]

(*iii*) The office supports 35 users on the packet-switched access link. What is the probability that exactly n users are transmitting simultaneously? [2 marks]

(*iv*) Find the probability that there are 11 or more users transmitting simultaneously. [3 marks]

(*v*) Describe an assumption about the nature of the traffic that underlies the answer to part (*b*)(*iv*) and give two examples of network traffic where this assumption is not valid. [3 marks]

7 Concurrent and Distributed Systems

(*a*) What is the relationship between *critical sections* and *mutual exclusion*? [2 marks]

(*b*) Describe how mutual exclusion can be achieved using:

(*i*) Spinlocks [2 marks]

(*ii*) Semaphores [2 marks]

(*iii*) Event Counts and Sequencers [2 marks]

(*c*) Describe the operation of a *monitor*. Be sure to explain how it supports mutual exclusion and *condition synchronization*. [6 marks]

(*d*) Why are monitors used in preference to *conditional critical regions*? [2 marks]

(*e*) In an effort to promote diversity, the Master of Holy Rock College, Cambridge, decides that the JCR must always hold at least one state school educated (SSE) student for every three public school educated (PSE) students. Reasoning that students are not very dissimilar from threads, he suggests the following entry and exit routines be followed:

```
JCR = new Semaphore(0);
```

```
/* for SSE threads */
enterRoom() {
  signal(JCR, 3);
}

leaveRoom() {
  wait(JCR);
  wait(JCR);
  wait(JCR);
}
```

```
/* for PSE threads */
enterRoom() {
  wait(JCR);
}

leaveRoom() {
  signal(JCR, 1);
}
```

We can assume that undergraduates are smart enough not to try and enter the JCR when it is full. Yet despite this, the Master's solution does not work quite as hoped! Describe what can go wrong, and suggest a fix. [4 marks]

8 Concurrent and Distributed Systems

(*a*) In the context of concurrent systems, what is a *transaction*? [1 mark]

(*b*) Describe the ACID properties of transactions. [4 marks]

(*c*) Compare and contrast *strict* and *non-strict* isolation. [2 marks]

(*d*) For each of the following, describe how it can be used to provide isolation and/or strict isolation:

(*i*) 2-Phase Locking (2PL) [3 marks]

(*ii*) Time-Stamp Ordering (TSO) [3 marks]

(*iii*) Optimistic Concurrency Control (OCC) [3 marks]

(*e*) A researcher suggests an isolation scheme that works as follows:

(*i*) Every object o has an associated version number, $V(o)$.

(*ii*) When executing, a transaction reads a copy of any object it wishes to access, and remembers the version number.

(*iii*) If the transaction wishes to modify an object, it modifies the copy rather than the original.

(*iv*) When complete, the transaction checks the versions of all objects it has modified; if any are different, it aborts; otherwise it writes back the new versions of all objects, incrementing their version numbers, and commits.

Assuming that step (*iv*) occurs atomically, does this scheme ensure serializability? Justify your answer. [4 marks]

9 Concurrent and Distributed Systems

(*a*) Many distributed systems make use of replication.

(*i*) Give *two* advantages and *one* disadvantage of using replication. [3 marks]

(*ii*) Distinguish *weak consistency* and *strong consistency*. What is the primary disadvantage of using the latter? [3 marks]

(*iii*) Describe how to commit a transaction in a distributed transaction processing system in which objects are replicated on different servers. [4 marks]

(*b*) Group communication can be achieved via *ordered multicast*. Describe how you would build an ordered multicast system which preserves *causal ordering*. [6 marks]

(*c*) You are part of a team tasked with building a distributed filing system. One of the requirements is that it must be possible to revoke access rights to a file within T milliseconds ($T \geq 0$). Describe how you could achieve this, commenting on how the value of T would influence your decision. [4 marks]

END OF PAPER