2011 Paper 8 Question 3

Comparative Architectures

(*a*) Why might a branch target buffer provide a poor prediction of procedure return addresses and what hardware solution may be employed to improve the accuracy of such predictions? [4 marks]

(*b*) What challenges must be overcome in order to achieve high instruction fetch rates for wide-issue superscalar processors? [6 marks]

(*c*) Embedded processors often allow both 16-bit and 32-bit instructions to be used in the same program. Why might this be advantageous? [4 marks]

(*d*) Branch prediction and speculative execution are often used to expose greater amounts of instruction-level parallelism in superscalar processors. A *reorder buffer* or *unified register file* may be used to help recover after mispredicted branches are detected.

(*i*) How are an instruction's operands located when a reorder buffer is used? [3 marks]

(*ii*) What actions are taken to recover from a mispredicted branch when a unified register file is used? [3 marks]