2010 Paper 8 Question 13

System-on-Chip Design

(*a*) Briefly describe polling, interrupt-driven I/O, and DMA in the context of a system-on-chip where the I/O device is connected to the same local bus as its controlling processor. [3 marks]

(*b*) What complexity and performance issues arise for each of the three techniques of part (*a*) when the I/O device is attached to a remote bus? [4 marks]

(*c*) Two processors in a system-on-chip communicate using a hardware packet channel that conveys fixed-length messages of 48 bytes.

(*i*) Draw or describe a suitable programming model for an end point that uses interrupts but no DMA. [4 marks]

(*ii*) Sketch assembly or C-like code for the transmit side of a suitable interrupt service routine that uses a circular buffer in local RAM or similar. [4 marks]

(*iii*) A high-level model of the channel is needed as part of a system simulation that uses blocking TLM (transactional level modelling). Sketch the core code of a suitable model using constructs from SystemC and the TLM 2.0 standard or some similar library. [3 marks]

(*iv*) Explain the relationship between the firmware fragment of your assembly code in part (*ii*) and your high-level model in part (*iii*). When and how would they ever interact? [2 marks]