2009 Paper 9 Question 8

System-on-Chip Design

Unless otherwise stated, use any appropriate combination of text, diagrams, SystemC and/or Register Transfer Language (RTL) code in your answers.

(a) Give a programming model for a simple DMA (direct memory access) controller with one control/status register and three operand registers: for block length, source address and destination address.
[The DMA controller, when active, becomes a bus master and copies a block of data from one area to another.] [4 marks]

(b) Give the precise condition for your DMA controller to generate an interrupt. [2 marks]

(c) Sketch the implementation (in C and/or assembly language) for a general-purpose block-copy function that uses the DMA controller. Include the steps of enabling and disabling interrupts. Assume all copies are an integer number of words and are word-aligned. [4 marks]

(d) Give a programming model for an audio sub-system that includes a modified DMA controller that is dedicated to copying audio samples to and from a sound codec (ADC (Analogue/Digital Converter) and DAC (Digital/Analogue Converter) pair). [6 marks]

(e) How must the buffering in the audio-subsystem of part (d) be dimensioned and how are interrupts used to maintain continuous streams of audio at the correct sample rate? [4 marks]