2008 Paper 3 Question 1

ECAD

(*a*) For the two mystery Verilog modules below, what output sequences do they produce assuming that registers are initially reset to zero? Explain your answer.   [6 marks]

```
module mystery0(input a, output reg [4:0] b);
  always @(posedge a) begin
    b[0] = !b[0];
    b[1] = b[0]     ^ b[1];
    b[2] = &b[1:0] ^ b[2];
    b[3] = &b[2:0] ^ b[3];
    b[4] = &b[3:0] ^ b[4];
  end
endmodule

module mystery1(input c, output reg [4:0] d);
  always @(posedge c)    d[0] <= !d[0];
  always @(posedge d[0]) d[1] <= !d[1];
  always @(posedge d[1]) d[2] <= !d[2];
  always @(posedge d[2]) d[3] <= !d[3];
  always @(posedge d[3]) d[4] <= !d[4];
endmodule
```

(*b*) If the modules were to be implemented in terms of two-input AND, OR and XOR gates, NOT gates, and D flip-flops, what would be the minimal circuits?   [6 marks]

(*c*) Which module could be clocked most quickly if it were implemented on an FPGA with 4-input look-up tables (LUTs)? Explain your answer.   [4 marks]

(*d*) What are the timing issues for any circuit looking at the outputs of the two mystery modules?   [4 marks]