2006 Paper 5 Question 2

Computer Design

(*a*) Why do pipelines exhibit branch and load delays? [6 marks]

(*b*) What impact does pipeline length have on clock frequency? [4 marks]

(*c*) Why might a shorter pipeline result in a more power-efficient design? [4 marks]

(*d*) Recently we have seen microprocessor manufacturers release dual-processor chips where each processor has a shorter pipeline than the earlier single-processor per chip designs. What sort of applications might run better on the older chips and *vice versa*? [6 marks]