2005 Paper 3 Question 1

ECAD

(a) What input condition will cause a D flip-flop to go metastable? [3 marks]

(b) What timing parameters have to be adhered to in order to avoid metastability? [3 marks]

(c) Will a D flip-flop remain in the metastable state indefinitely? [3 marks]

(d) What is the difference between synchronisation and debouncing? [3 marks]

(e) How is a synchroniser made out of D flip-flops? [3 marks]

(f) What are the failure modes for the following two counters (`count0` and `count1`) if `asyncInput` comes from a synchronous digital circuit clocked from a different clock source and `keyInput` comes directly from a mechanical push button?

```
reg [63:0] count0, count1;
reg [2:0]  sync;
always @(posedge clock)
  begin
    // count how many clock cycles asyncInput is high
    if(asyncInput) count0 <= count0+1;
    // count the number of times the keyInput is pressed
    sync <= {sync[1:0],keyInput};
    if(!sync[2] && sync[1]) count1 <= count1+1;
  end
```

[5 marks]