2004 Paper 8 Question 2

VLSI Design

(*a*) Sketch the circuit of a dynamic CMOS gate controlled by a clock φ that precharges when $\varphi = 0$ and evaluates the function $\overline{A + B \cdot C}$ when $\varphi = 1$. [4 marks]

(*b*) Explain how your circuit works and describe *two* advantages and *two* disadvantages when compared with static CMOS. [6 marks]

(*c*) Present *two* ways of designing cascaded logic in dynamic CMOS and explain how they work. [8 marks]

(*d*) Present a further modification to the circuit so that its output is retained when the clock stops. [2 marks]