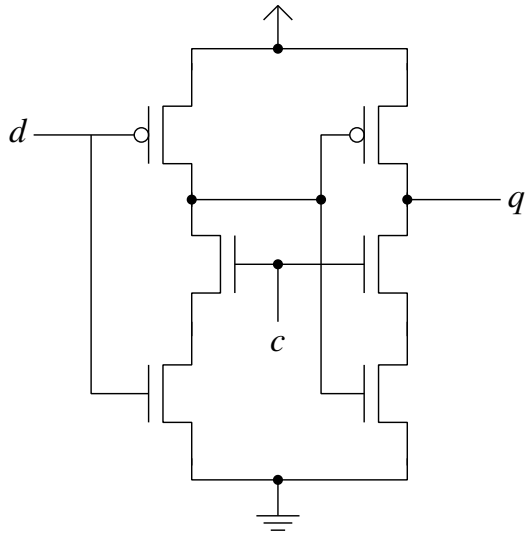
2001 Paper 9 Question 2

VLSI Design

(*a*) Give transistor level designs for 2-input NAND gates using static and dynamic CMOS, explaining how the latter is controlled by a clock. [8 marks]

(*b*) Comment on the relative merits of static and dynamic logic for evaluating more complicated combinatorial functions, including transistor count, wiring complexity, speed and implications for cascaded logic. [4 marks]

(*c*) Consider the following circuit for a dynamic latch:



Specify the input and output signals, and explain its operation carefully. [8 marks]