## 2001 Paper 2 Question 3

## Digital Electronics

Consider two numbers $X$ and $Y$, each represented by $n$ boolean variables $x_{n-1} x_{n-2} \ldots x_{0}$ and $y_{n-1} y_{n-2} \ldots y_{0}$ in the usual way so that for example $X=\sum_{i=0}^{n-1} 2^{i} x_{i}$.
(a) Design a full adder to find $Z=X+Y$ in the case where $n=2$. If each gate has a delay $\tau$, how quickly is the result of the addition available after the inputs are presented?
(b) Estimate a rough upper bound on the number of gates required to build a full adder in combinational logic when $n=4$.
(c) Describe two techniques for building adders which reduce gate count.
(d) Design a full multiplier to find $W=X \times Y$ for the case where $n=2$. [5 marks]

